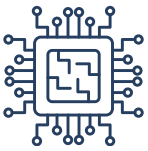
www.barcelona-zettascale-lab.es

BARCELONA **ZETTASCALE** LAB

The design of RISC-V based advanced chips, including RISC-V processor + VPU + high-performance memory hierarchy



High-Tech Prototypes

Development of chip prototypes based on RISC-V for impacting in the next generation of European supercomputers

Strategic Partnerships

Collaborating with leading European and international companies and partners in semiconductors

Strengthening the Software Ecosystem

Ensuring RISC-V compatibility and maximizing the performance of these new designs

Advancing European Technological Sovereignty

Reducing European's dependence on HW technologies and strengthening European's capacity to produce critical technologies

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This initiative is aimed to position Spain as a leader in the design and development of advanced architectures, as part of a broader strategy including the PERTE Chip.

BSC Barcelona Supercomputing Center
Centro Nacional de Supercomputación

This project is promoted by the Spanish Ministry for Digital Transformation and the Civil Service, within the framework of the Recovery, Transformation and Resilience Plan – Funded by the European Union – NextGenerationEU.

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GOBIERNO DE ESPAÑA
MINISTERIO PARA LA TRANSFORMACIÓN DIGITAL Y LA FUNCIÓN PÚBLICA
SECRETARÍA DE ESTADO DE TELECOMUNICACIONES E INFRAESTRUCTURAS DIGITALES

Plan de Recuperación, Transformación y Resiliencia