BARCELONA **ZETTASCALE** LAB

Hacia el Zettascale: Avances del Barcelona Zettascale Lab

Evento Final del proyecto BZL Madrid (España)
16 de Junio de 2026

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

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Conclusiones, siguientes pasos, ruegos y preguntas

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Results: Achievements (conclusions)

- Achieved **main objectives** of the Project
  - Design, implementation, verification and fabrication of two test chips
    - Cinco Ranch TC1 (single core)
    - Cinco Ranch TC2 (dual core)
  - Development of an entire SW stack for the RISC-V designs at BSC
  - Validation by means of meaningful use-cases

- Creation of an **academic hub** for talent attraction and creation in chips design and RISC-V software
  - Bridge between university and European industry
  - Industry-inspired methodologies
  - Capacity to design HPC+AI chips in advanced technology nodes

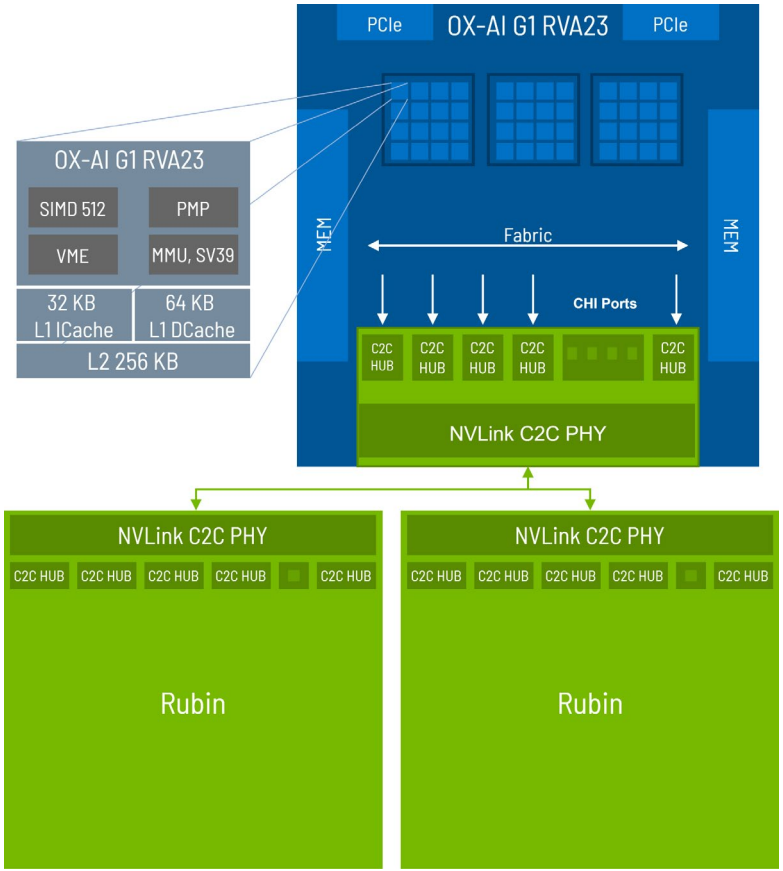
Impact: Outcomes and Future work

- **Project outcomes:** DARE, HIGHER, MicroNanoSpain, Cátedras PERTE Chip, ODE4EC, "BZLx",…
  - Better methodologies, infrastructures, and expertise
  - Potential technology transfer to local industry

- **Future work**
  - New hardware design and implementations (TC3, …)
  - OS/SDV support for next-generation RISC-V hardware platforms
  - Further optimizations for Compilers (e.g. RVV), Runtimes (e.g., programming models), Libraries (e.g., numerical) and Frameworks (e.g., AI/ML)
  - Large scale evaluation on multi-node systems (the network leap)

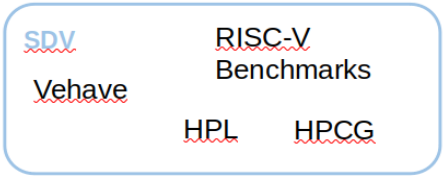
Towards Cinco Ranch Test Chip 3

- Target **CPU-GPU platform** based on the next generation of NVIDIA GPUs
- Multi-core System-on-Chip (SoC) based on Lagarto Ox and the Network-on-Chip (NoC) developed by BSC in the BZL and DARE project. This enables:
  - **Efficient** execution of AI and HPC apps
  - Coherent cache hierarchy based on the AMBA CHI standard
  - Advanced PCIe and LPDDR controllers and PHY's optimized for **Intel 18A**
- Target: 16- core design in 48mm2 that scales to 64-256 with more silicon area



BSC Software Development for TC3

- A complete HPC and AI software stack developed at BSC and deployed across Europe
- Over 150 software engineers developing compilers, mathematical libraries, and offloading mechanisms for CPU+GPU nodes
- Extend and deploy BSC software ecosystem in the node and rack systems as part of the joint collaboration.
- This software ecosystem will blend open-source software developed by BSC and European partners over several decades of European-funded software projects as well as NVIDIA rich software stack (CUDA)



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THANKS

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