



BARCELONA ZETTASCALE LAB

Hacia el Zettascale: Avances del Barcelona Zettascale Lab

Evento Final del proyecto BZL Madrid (España)
16 de Junio de 2026



**Barcelona
Supercomputing
Center**
Centro Nacional de Supercomputación



BARCELONA ZETTASCALE LAB

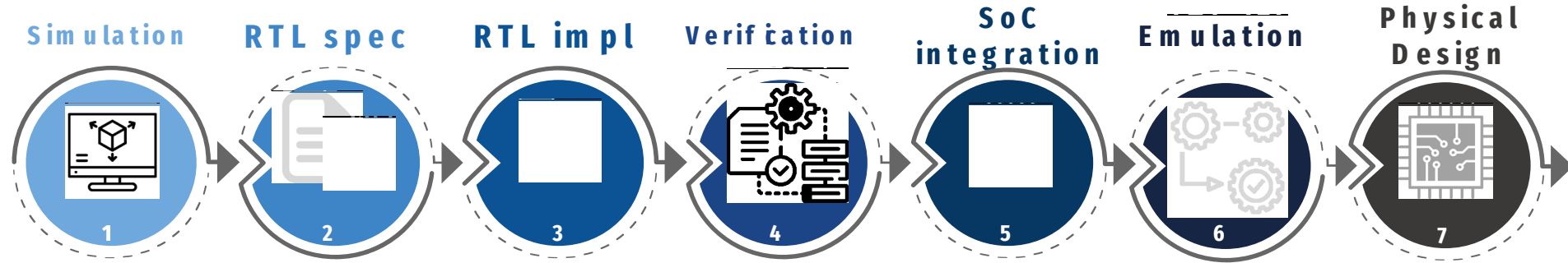
Avances en la Arquitectura de Computadores de BZL

Miquel Moretó – BSC

Evento Final del proyecto BZL Madrid (España)
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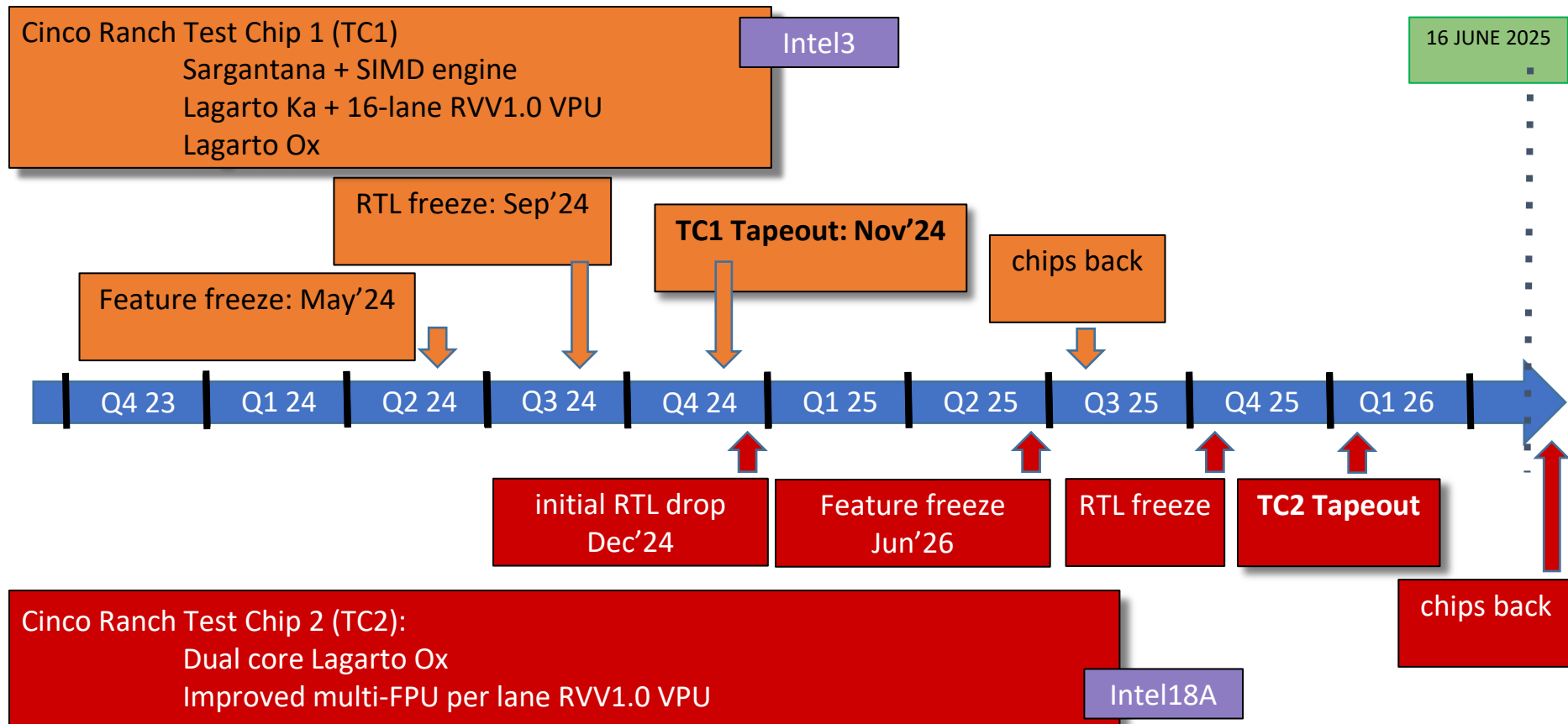


BZL Chip Design Organization



- Create new engineering teams specialized in the different stages of a chip design
- Incorporate industry best practices in the chip design methodology at BSC (Intel and other collaborators in European projects)
- Automation (DevOps) and periodic quality assessment reviews

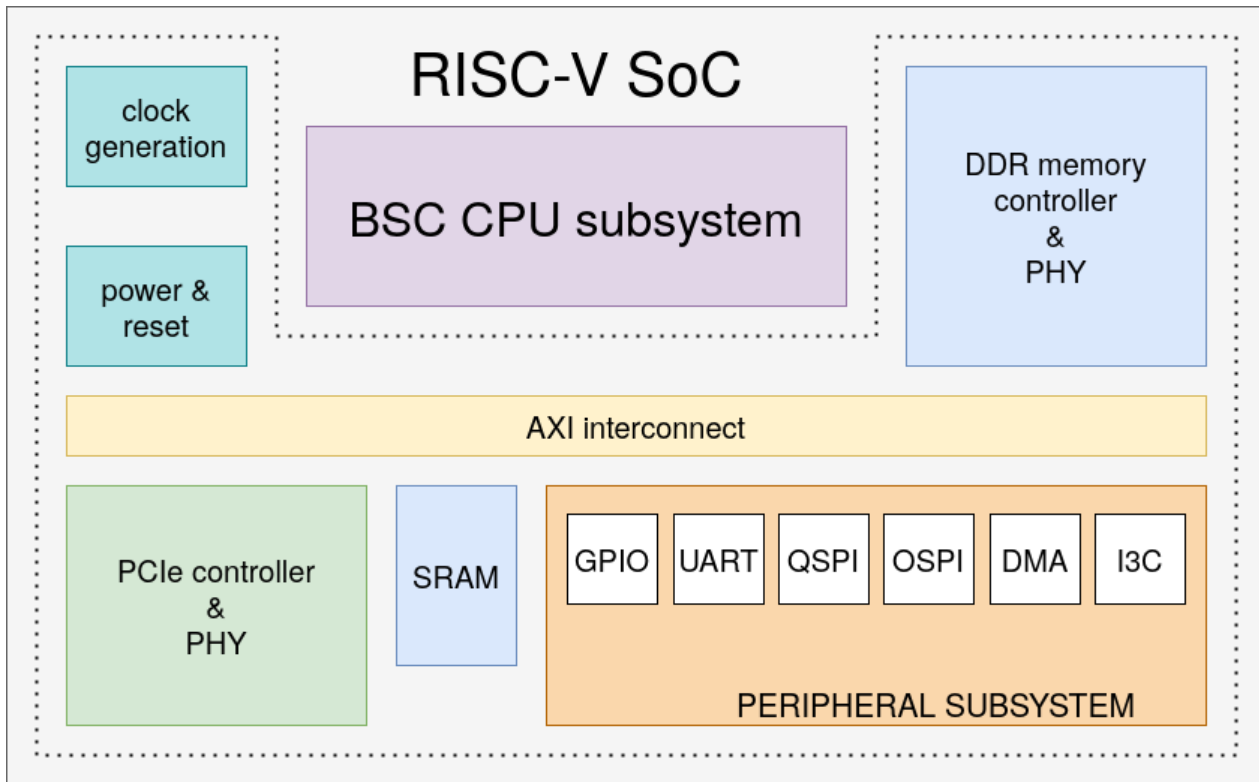
BZL Tapeouts Timeline



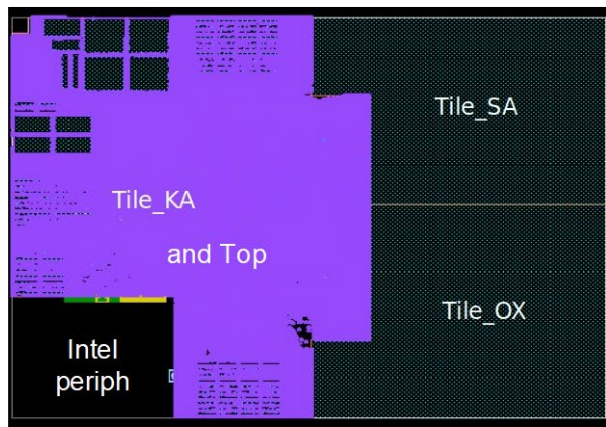
Cinco Ranch Test Chip 1



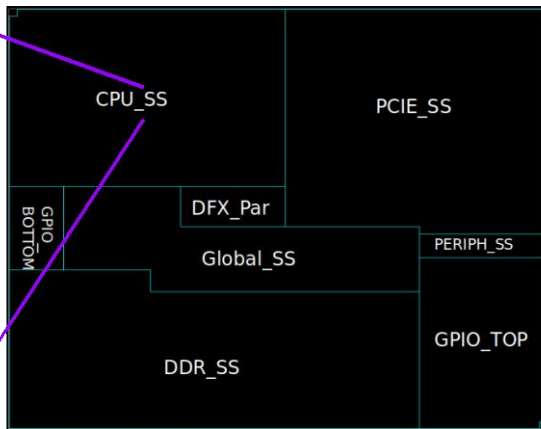
- Single core design with 3 different cores selected at boot time
 - Sargantana in-order single-issue RV64G with custom extensions for genomics sequence alignment
 - Lagarto Ka dual-issue out-of-order with a 16-lane Vitruvius RVV1.0 VPU
 - Lagarto Ox 6-way out-of-order RV64GC
- Tech. node: Intel3



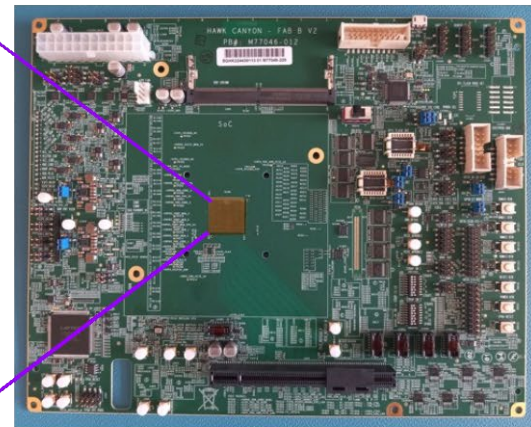
Cinco Ranch Test Chip 1



BSC cpu subsystem



CincoRanch TC1 chip



Hawk Canyon platform

- Area (Intel3):
 - CPU: 3.2mm²
 - Die size 4,05mm * 3,75mm (15,2mm²)
- Submitted for fabrication in Nov 2024
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- Boards received in Jan 2025 (without chips)
- Intel received chips in the end of May
- Chips expected at BSC in the end of June
- Bring-up during July-Sept 2025
- Successful Linux boot!!

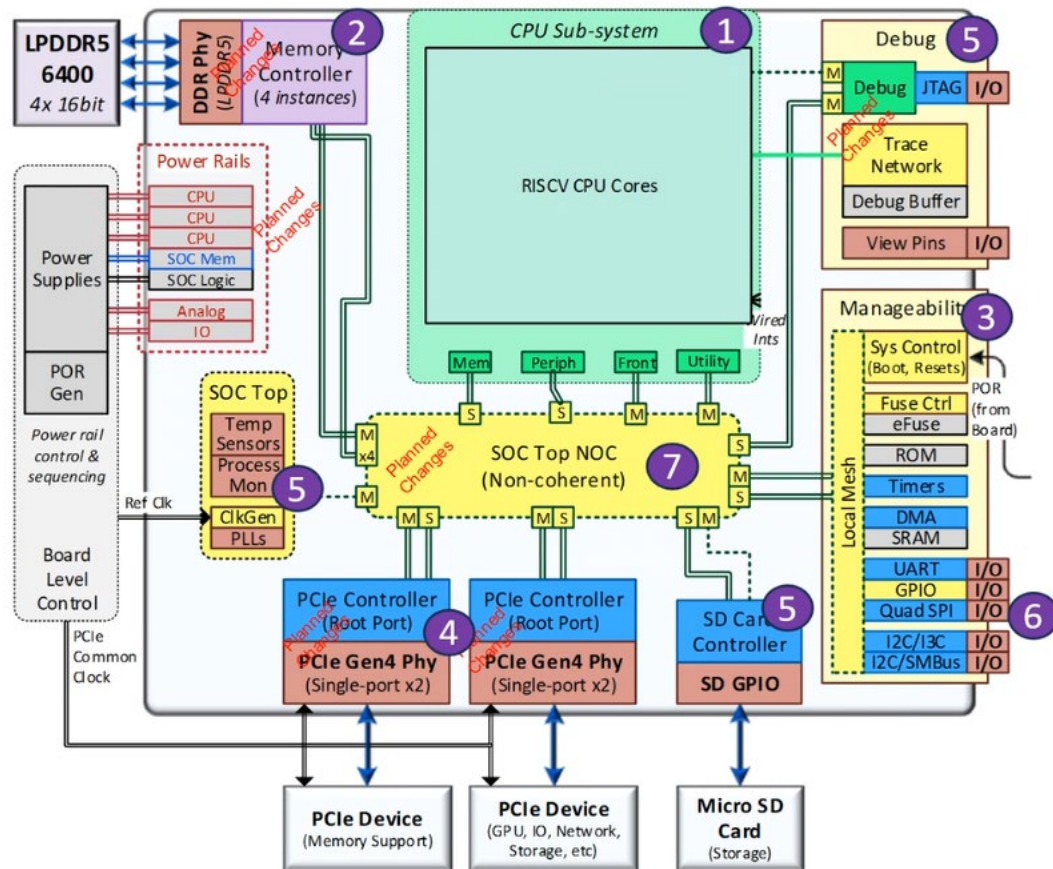
Cinco Ranch TC1 Board



Cinco Ranch Test Chip 2



- Very similar top-level IPs with increased performance
- Increased memory BW
- New technology node: **Intel 18A**
- More area: 12x4mm² (die), ~5mm² (BSC), ~12mm² (OCT)
- **Access to PDK!**
- AXI5 interface with CPU
- New address mapping



The diagram illustrates the architecture of the Lagarto OX processor, organized into four main functional blocks: Front End, Scheduling Engine, Execution FUs, and Load/Store Unit.

Front End

- FTQ** (Fetch Target Queue) feeds into the **RAS (32-entries)**.
- RAS (32-entries)** includes **2BCDSKEW** and **512-entries BTB**.
- ITLB (32-entries)** and **L1 I-Cache (16-KiB 4-Way)** provide instructions at **64B/Cycle**.
- Fetch & Predecode (3 Cycles)** can handle **Upto 8 Insts/Cycle**.
- Instruction Fusion Detector & μOps Generation** feeds into the **Fetch Instruction Buffer (32-entries)**.
- Fetch Instruction Buffer (32-entries)** feeds into the **6-way Decoder with 5 fusion idioms**.
- 6-way Decoder with 5 fusion idioms** feeds into the **Rename/Dispatch** block.
- Rename/Dispatch** handles **6-Scalar Instructions per cycle** and **4/2-Vector per per cycle**.

Scheduling Engine

- ROB (256 entries)** (Reorder Buffer) is the central component.
- ACC Interface** feeds into the **ROB**.
- Vector Slicer IO** feeds into the **ROB**.
- Non-Scheduling Queue** (three instances) feeds into the **ROB**.
- RF Port Scheduler** feeds into the **ROB**.
- SIMD RF (128-entries)**, **INT RF (256-entries)**, and **FP RF (256-entries)** feed into the **ROB**.
- SIMD IO (32 entries)**, **INT IO (48 entries)**, **MEM IO (32 entries)**, and **FP IO (32 entries)** feed into the **ROB**.
- L2 Cache (128-KiB 4-way)** and **64-MSHR** (Miss Status Holding Register) are connected to the **ROB**.

Execution FUs (Functional Units)

- ALU BRU** (Arithmetic Logic Unit Branch/Reduce Unit) - two instances.
- ALU DIVU** (Arithmetic Logic Unit Divide Unit) - two instances.
- SIMD S12 INT/FP** (SIMD Scalar 128-bit Integer/Float) - two instances.
- VAGU** (Vector Arithmetic General Purpose Unit) - two instances.
- AGU ST-DATA** (Address Generation Unit Store/Data) - two instances.
- fpFMA fpNONCOMP fpDIVSORT fpCONV** (Floating Point Fused Multiply-Add, Non-Commutative Multiply-Add, Divide/Sort, and Convert) - two instances.

Load/Store Unit

- ACC MEM Interface** feeds into the **Store Manager**.
- Store Manager** feeds into the **Load Store 0 (64-entries)** and the **Store Buffer (32-entries)**.
- Load Store 0 (64-entries)** and **Store Buffer (32-entries)** are connected via **8B/cycle** bidirectional links.
- Load Data Buffer** feeds into the **Load Store 0**.
- LSO Arbitrer** (Load Store Order Arbitrer) is connected to both **Load Store 0** and **Store Buffer**.
- L1 DTLB (64-entries)** and **PTW 8-MSHR** (Page Table Walk 8-MSHR) feed into the **L1 D-Cache (32-KiB 4-way)**.
- L1 D-Cache (32-KiB 4-way)** and **64 MSHRs** are connected to the **L2 Cache (128-KiB 4-way)** at **64B/Cycle**.

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Cinco Ranch TC2 Board



THANKS



Este proyecto está financiado por el Ministerio para la Transformación Digital y de la función pública, en el marco del Plan de Recuperación Transformación y Resiliencia – y la Unión Europea – NextGenerationEU. Los puntos de vista y las opiniones expresadas son únicamente los del autor o autores y no reflejan necesariamente los de la Unión Europea. Ni la Unión Europea ni la Comisión Europea pueden ser consideradas responsables de las mismas.



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