BARCELONA **ZETTASCALE** LAB

Cómo ganar experiencia en RISC-V con el proyecto BZL

Tutorial - Jornadas SARTECO
16 de Junio de 2026

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

Before starting

Requirements for following the hands-on:

- Gem5 session:

```
docker run -it --rm registry.gitlab.bsc.es/aarmejac/gem5-handson
```

Agenda - Tutorial BZL

- **11:00 – 11:30h:** Introducción al proyecto BZL
  - R. Ignacio Genovese
- **11:30 – 14:00h**: Cómo simular y analizar resultados con Gem5
  - Iván Fernández
- **14:00 - 15:00 Lunch Break**
- **15:00 – 16:30h**: Introducción a los diseños avanzados de BZL y acceso a la infraestructura
  - Daniel González
- **16:30 - 17:00h Coffee Break**
- **17:00 – 18:35h:** Cómo ejecutar aplicaciones en diseños avanzados de BZL
  - Daniel González
- **18:30 – 18:35h:** Conclusión y cierre
  - Miquel Moretó

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Introducción a RISC-V

Evento Final del proyecto BZL Madrid (España)
16 de Junio de 2026

Barcelona Supercomputing Center
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The Instruction Set Architecture Landscape

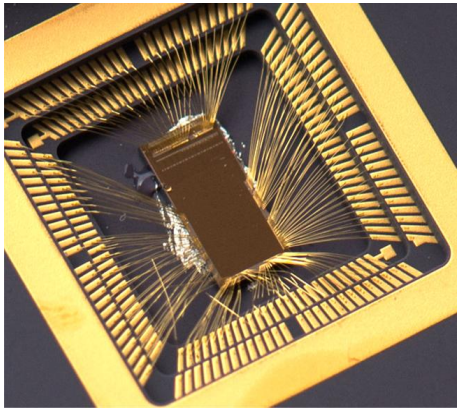
	intel	arm	RISC-V
Design Philosophy	CISC	RISC	RISC
Governance & Licensing	Closed (Proprietary IP)	Closed (IP Licensing Fees)	Open Standard (Royalty-Free)
Extensibility	Locked	Locked	Modular (Custom User Extensions)
Primary Hardware Domains	Desktop & Enterprise Server	Mobile & Microcontrollers	Ubiquitous & Workload-Specific (HPC, AI)

RISC-V is the industry standard ISA that **expands opportunity**

Global standards are a catalyst to accelerate technical innovation

Standards have been critical to innovation & tech adoption for decades

Standards create access to opportunities for a wide range of stakeholders

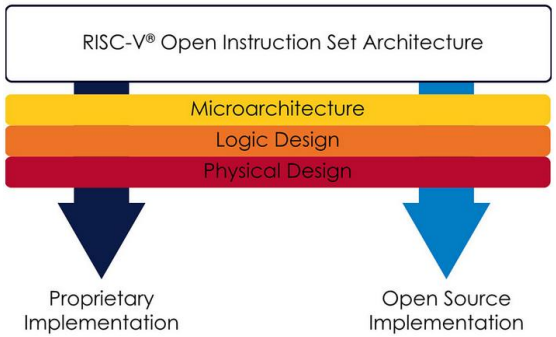


RISC-V is a standards-defined Instruction Set Architecture developed by a global community

- ✅ **Open-standard & Royalty-free**
- ✅ **Used in real chips and systems**
- ✅ **Gaining global support across OSes and industries**

What is RISC-V?

- **An open Instruction Set Architecture (ISA) standard**
  - Based on Reduced Instruction Set Computing (**RISC**) principles
  - Standardisation activities driven by expert members
  - Targeting multiple areas from HPC & ML to the data centre to embedded computing
    - Additional extensions, tools and resources
- **Why is RISC-V interesting for HPC?**
  - Freely develop new technologies based upon RISC-V
  - Standards community driven
  - Modular design of ISA
    - Pick and mix parts that you need
    - From low power embedded devices to HPC and IA accelerators



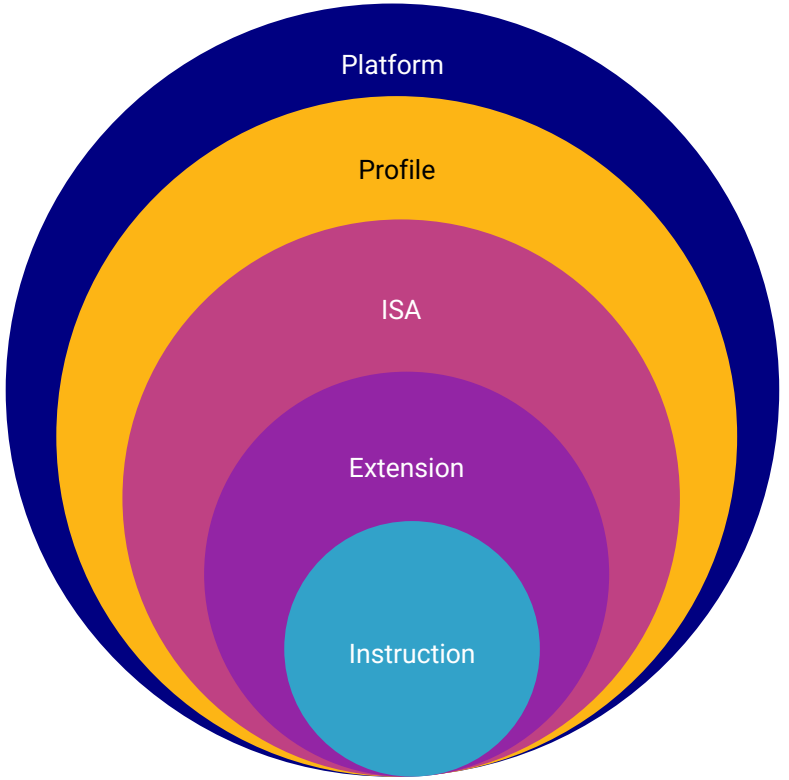
RISC-V Principles

RISC-V was designed to provide a highly **modular and extensible instruction set** and includes a large and growing set of standard **extensions**, where each standard extension is a bundle of **instruction-set features**.

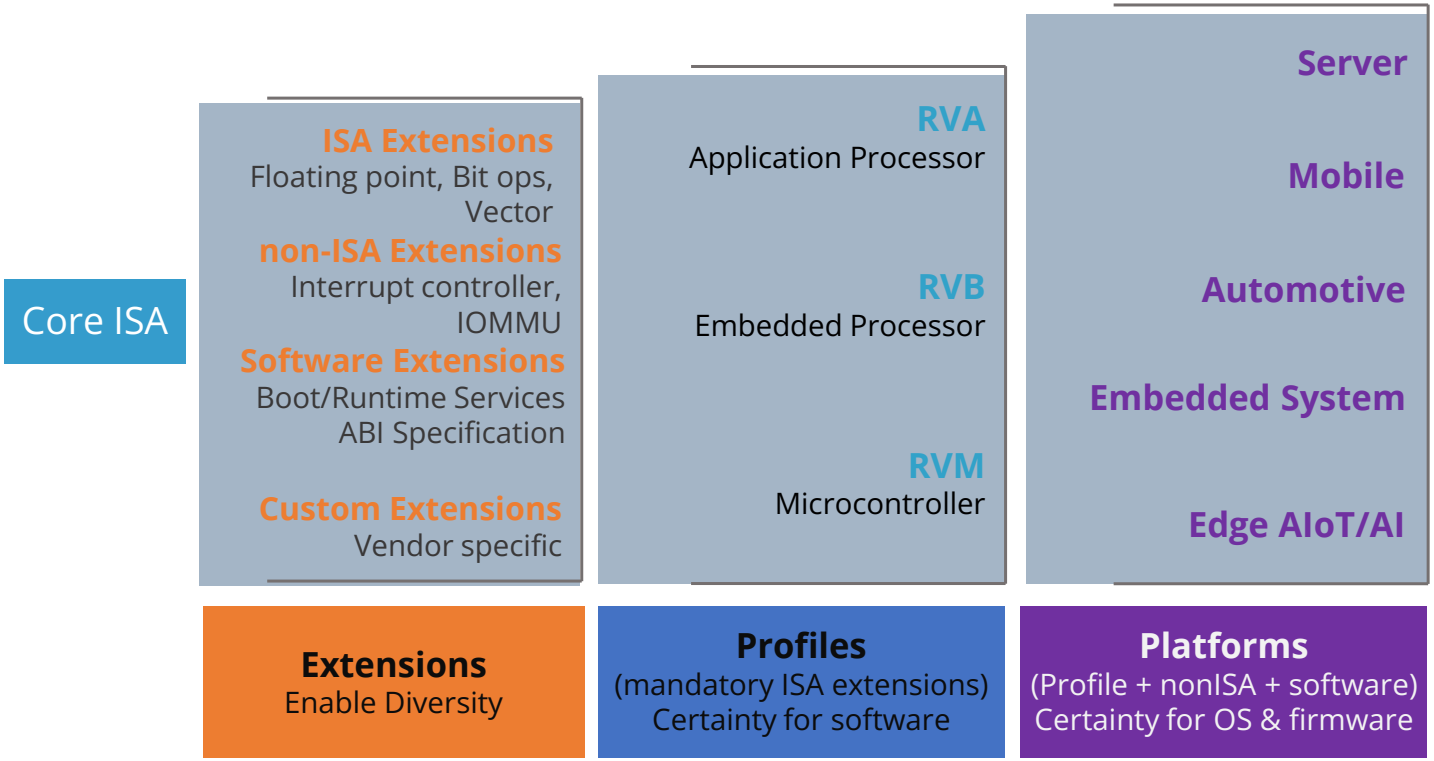
- **Unlike other ISAs:**
  - RISC-V has a broad set of contributors and implementers.
  - RISC-V allows users to add their own custom extensions.
- **How to organize the information?**
  - Instruction → Extension → ISA → Profile → Platform

RISC-V Basic Concepts

- **Instruction:** Language of the computer ~ word
- **Extension:** group of instructions that add further functionality to the base architecture
- **Instruction Set Architecture (ISA):** List of processor commands in machine language
- **Profile:** set of common ISA extensions together (Mandates + Options)
- **Platform:** set of specs for building real hardware platforms/systems (procedures, boot process,...)



Profiles, Platforms and software ecosystem



Big Data, Database, LLM

Red Hat Enterprise Linux · Canonical Ubuntu · SUSE

Android Apps
Android

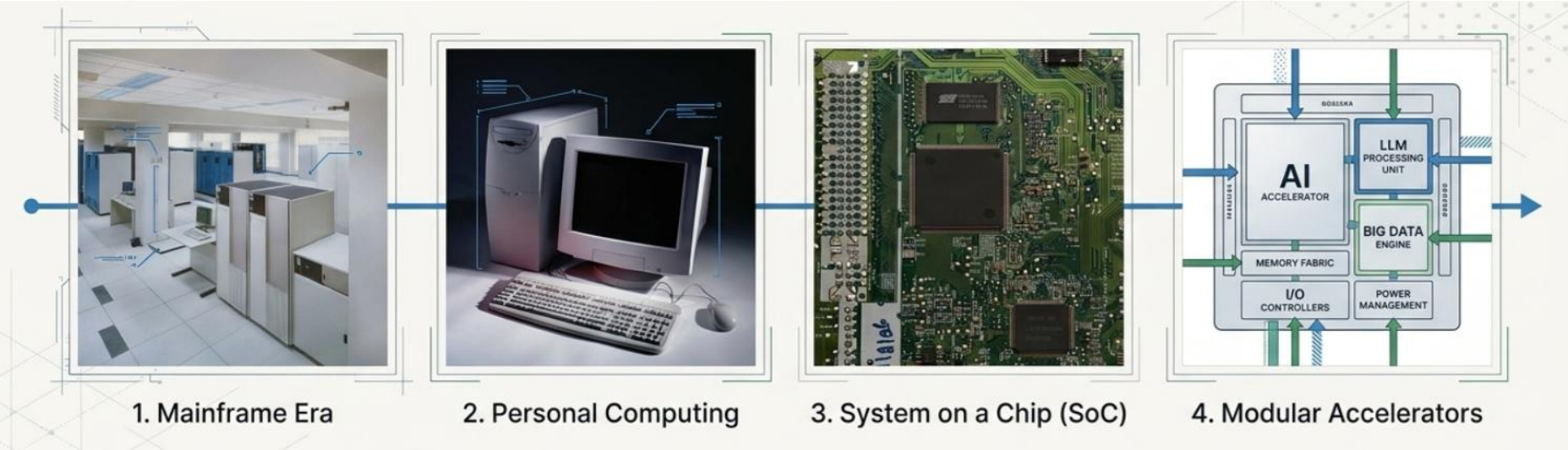
Android Auto
Safety Linux

Automotive Grade Linux

yocto PROJECT
Container runtime

Zephyr · FreeRTOS

Entering the Era of Workload-designed Silicon



Standardized monolithic hardware is no longer sufficient for modern HPC and ML workloads.

The future requires specialized, modular silicon.

RISC-V matters. It is a game changer.

Country

- Invest locally and **impact globally**
- Incubate technology **ecosystem** from research to industry
- Access **worldwide** market

Multinational

- **Control** strategic roadmap
- New **opportunities** for innovation and influence
- **Growth** business models

Research

- Accelerate local **innovation** and **talent**
- Access **global** RISC-V research **network**
- Tech transfer **addressing real world applications**

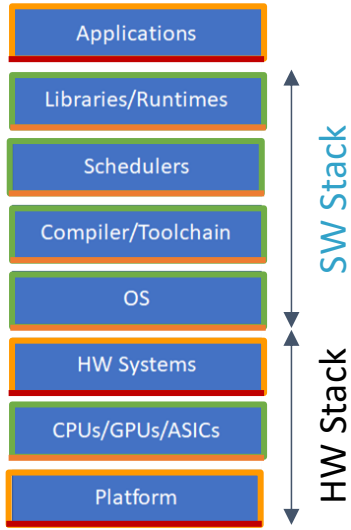
Start-ups

- Supercharge hardware and software **co-design**
- **No vendor lock-in**
- **Collaboration** partners

RISC-V an open standard from/for the

- **RISC-V Ecosystem landscape**
  https://landscape.riscv.org/

- **RISC-V whole stack**



RISC-V HPC adoption

- 35% of application runtime required for HPC are available for RISC-V
- New performance RVA23 hardware to speed adoption
- NVIDIA porting CUDA to RISC-V
- Availability of HPC-centric RISC-V accelerators from Tenstorrent, Inspire Semiconductor & Axelera AI
- Recent participation at SC25, HIPEAC & ISC25

RISC-V

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Centro Nacional de Supercomputación
epcc
UK National Supercomputing Centre
Meta
openchip
Enabling the Digital World
希姆计算
STREAM COMPUTING
NUCLEI
SiFive
E4
COMPUTER ENGINEERING
TCL Tactical Computing Labs
AKEANA
tenstorrent
达摩院
Alibaba DAMO Academy
SUSE
InspireSemi
semidynamics

RISC-V in HPC: The current status

- **Application support (based on commercial platforms)**
  - Lower performance than x86 for memory bandwidth or latency bound
- **Software tooling**
  - Compiler vectorization support
  - Compiler support for Fortran
  - Short on performance analysis tooling
  - Not enough performance counters
- **Infrastructure**
  - Low number of testbeds
  - Low maturity on high performance parallel filesystems (e.g., Lustre, and GPFS)
  - Management and Monitoring tools
  - Lack of support for high performance networking

REFERENCE: https://riscv-europe.org/summit/2025/media/proceedings/2025-05-13-RISC-V-Summit-Europe-P3.1.04-BROWN-abstract.pdf

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Visión General del BZL

Tutorial - Jornadas SARTECO
16 de Junio de 2026

CS mission and research directions

Mission - influence the way computational platforms targeting **HPC and AI** are:

Designed - Holistic Computer Architecture Research

Programmed - Innovating in Programming Models

Optimized & Used - Performance Analytics Tools: From data to insight

Research directions

1. European core and accelerator designs and implementations
2. Tools and methodologies for transitioning applications to new platforms
3. HPC programming and execution environments
4. AI research and cutting-edge applications
5. HPC and AI critical edge systems

450 researchers,
+25 research groups

HPC Architecture (HPCArch) Research Area

4

Research groups

- Computer Arch. for Parallel Paradigms
- High-Performance Domain Specific Arch.
- Memory Technologies
- Parallel Software for New Arch.

HPCArch Governance Board

6

Support Engineering groups

- Architecture Simulation
- Microarchitecture Design and Implementation
- Design Verification
- FPGA Technologies
- Synthesis and Physical Design
- Technical Management

4

Main projects to design, implement and fabricate EU cores and accelerators

European Processor Initiative

THE EUPILOT

Pilot using Independent Local & Open Technologies

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dare

Industry Contracts

Arm
IBM
Intel
Lenovo
Micron
OCT

Organization Contacts

RISC-V Int.
ESRA
OpenHW Foundation
AESEMI
MicroNanoSpain
SOHA
ETP4HPC

BZL Project Description

Project title: Barcelona Zettascale Laboratory (BZL)

Dates: 12/2022 – 06/2026 (3.5 years)

Main goal: Build first BSC-only HPC multicore design

RISC-V OoO processor + VPU Acc + High performance cache hierarchy

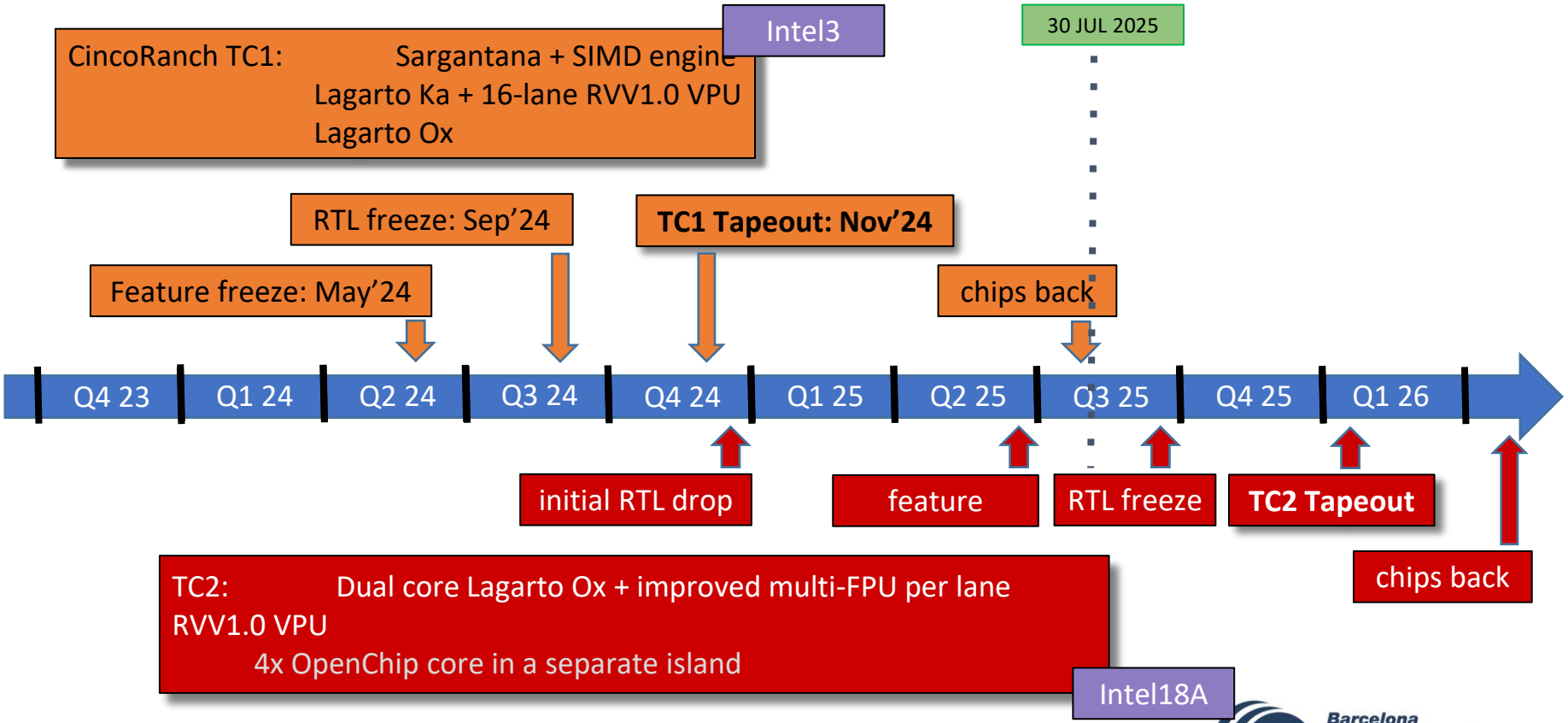
- Collaborate with Intel to fabricate such design
  - Two test chips with Intel Foundry Systems (IFS)
    - BZL Tapeout 1 (TC1) → Intel3
    - BZL Tapeout 2 (TC2) → Intel 18A
  - Intel provides technology-dependent IPs

Important milestones:

- Nov 2024: 1st tapeout with a reduced number of cores
- Jan 2026: 2nd tapeout with larger number of cores

Current BZL team has 175+ engineers among all teams

BZL Tapeouts Timeline



From Research to Production: Evolution of the Lagarto Family

- **Lagarto Hun (2019):** First design in TSMC 65nm; simple **in-order** execution, single issue.
- **Sargantana (2022):** Manufactured in GF 22nm; optimized efficiency for microcontroller applications.
- **Lagarto Ka (2022):** Introduced **out-of-order (OoO)** execution with dual-issue capability.
- **Lagarto Ox (2024-2026):** The core of TC2. A high-performance computing (HPC) processor with aggressive out-of-order execution and **4-instruction issue per cycle**.
- **Key Milestone:** TC2 represents the maturity of BSC's design team, moving from microcontrollers to high-performance processors capable of powering future supercomputers.

Vector Power: BZL's RVV 1.0 Accelerator

- **Standard Compliance:** Full adherence to the **RISC-V Vector (RVV) version 1.0** specification.
- **Architecture:** Optimized design with **4 floating-point functional units** per each of the **8 lanes**.
- **Performance:** Capable of performing **16 double-precision operations per cycle**.
- **Agnostic Vector Length:** Parameterized design supporting up to **16,384-bit VLEN**, ensuring software portability across different hardware implementations.
- **Efficiency:** Optimized inner loops in the VPU achieve performance levels exceeding **97% of the theoretical peak**.

TC2 SoC Block Diagram

Very similar top-level IPs as TC1 with <u>increased performance</u>

Increased memory BW

New technology node: Intel 18A

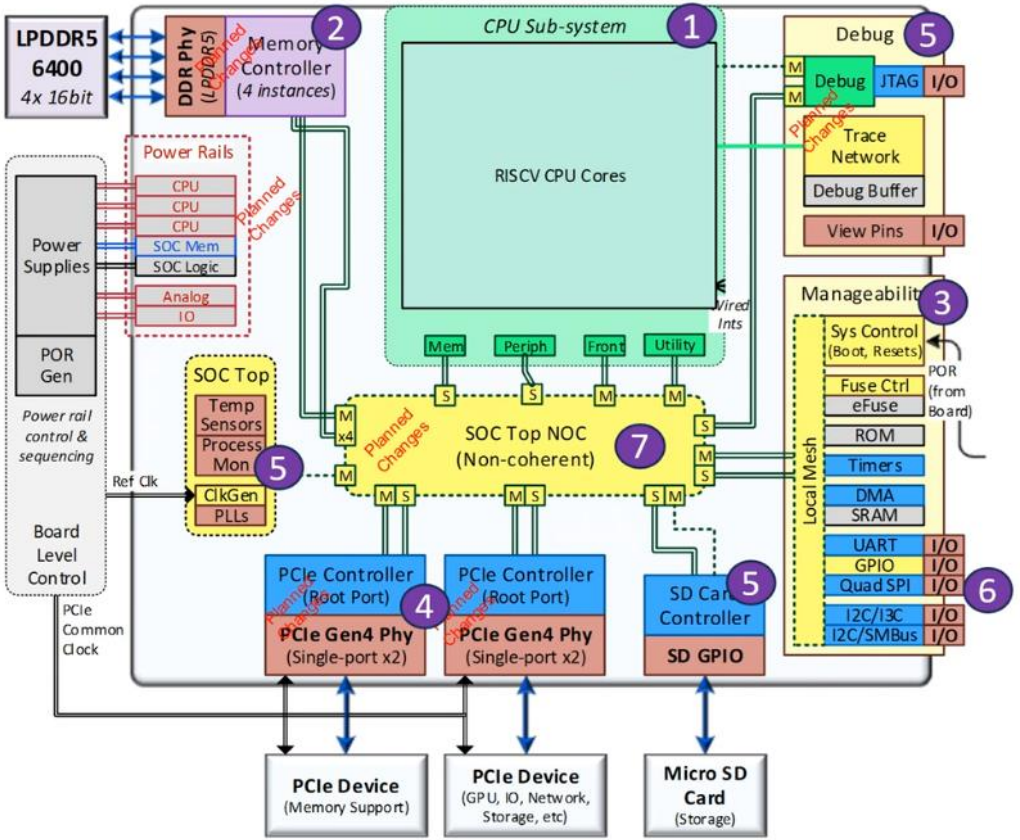
More area: 12x4 mm^2 (die)- 2 islands

~4 mm^2 (BSC) / ~12 mm^2 (OCT)

1 island active at a time - selection at power on

Single interface at Intel SoC - AXI Mux

AXI5 interface with CPU



Workflow: HW/SW co-design

FPGA-based emulation

Commercial RISC-V boards

HPC Software

Workloads

Libraries

Runtimes

OS

Compiler/Toolchain

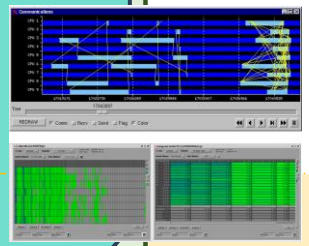
Performance Analysis

Behave

Paraver

Extrae

HW Counters



CO-DESIGN

HPC Architecture (HW)

Simulation 1

RTL 2

Verification 3

SoC integration 4

FPGA Emulation 5

Physical Design 6

Tapeout

GDS

Device PVT Characterization 7

Bring-up 8

SoC Functional Testing 9

SoC Performance Testing 10

Chip

PVT: Process-Voltage-Temperature

Monthly team hackathons!

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The BZL "Full Stack" Ecosystem

- **Software Development Vehicle (SDV):** Utilizing **Makinote FPGAs**, QEMU, and Gem5 to decouple software development from physical chip fabrication.
- **Operating Systems:** Robust support for booting **Linux**, with validated distributions including **Fedora, Ubuntu, and NixOS**.
- **Toolchain & Libraries:** LLVM and GCC compilers optimized for RISC-V auto-vectorization, integrated with numerical libraries like **BLIS/FLAME**.
- **Programming Models:** Native integration of **OpenMP, PyCOMPSs**, and task-aware libraries to fully leverage the VPU's capabilities.

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Roadmap: Project DARE and TC3 Vision

- **DARE Project (2025-2028):** Immediate successor with a €240M budget, focusing on **TSMC 4nm** technology and advanced matrix accelerators.
- **TC3 Evolution:** A vision for a **monolithic BSC-owned SoC** that eliminates reliance on third-party top-level IPs.
- **Platform Versatility:** Planning for two distinct platform variants:
  - **HPC-Oriented:** Maximizing chip area for computation (continuing the CincoRanch lineage).
  - **Desktop-Oriented:** Including full connectivity suites (Ethernet, storage controllers, etc.).
- **Ultimate Goal:** Achieving full **technological sovereignty** in high-end chip design within Spain and Europe over the next decade.

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Thank you

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Financiado por la Unión Europea
NextGenerationEU

MINISTERIO PARA LA TRANSFORMACIÓN DIGITAL Y DE LA FUNCIÓN PÚBLICA

SECRETARÍA DE ESTADO DE TELECOMUNICACIONES E INFRAESTRUCTURAS DIGITALES

Plan de Recuperación, Transformación y Resiliencia

Este proyecto se impulsa por el Ministerio para la Transformación Digital y de la Función Pública, en el marco del Plan de Recuperación, Transformación y Resiliencia - Financiado por la Unión Europea – NextGenerationEU

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