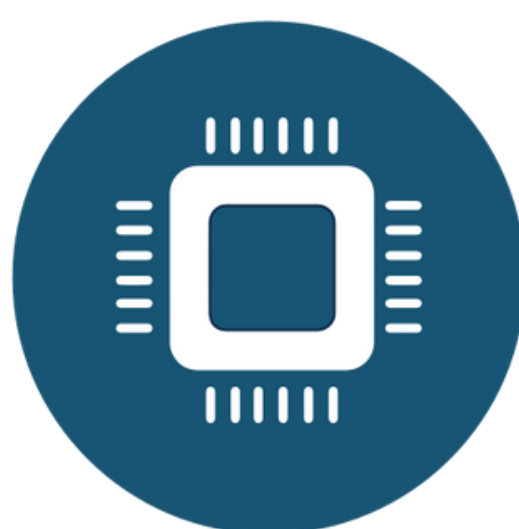




BARCELONA ZETTASCALE LAB

The BZL project focuses on the creation of high-performance multicore chip designs using the RISC-V infrastructure. This includes the integration of a RISC-V processor, a VPU accelerator, and an HPC cache hierarchy. There is close collaboration with Intel for the manufacturing of these designs. The hardware team, composed of more than 70 engineers, is divided into groups focused on simulation, RTL, verification, FPGA, physical design, and manufacturing.



Development of High-Tech Prototypes:

The project focuses on developing chip prototypes based on the RISC-V architecture, designed to be integrated into future European supercomputers.



Creation of a Compatible Software Ecosystem:

Alongside the hardware, a software ecosystem is being developed to ensure compatibility and maximize the performance of the new processors.



Promotion of sustainability and energy efficiency:

The lab will focus on sustainability by looking for solutions to promote energy efficiency and circular economy.



Collaboration with Strategic Partners:

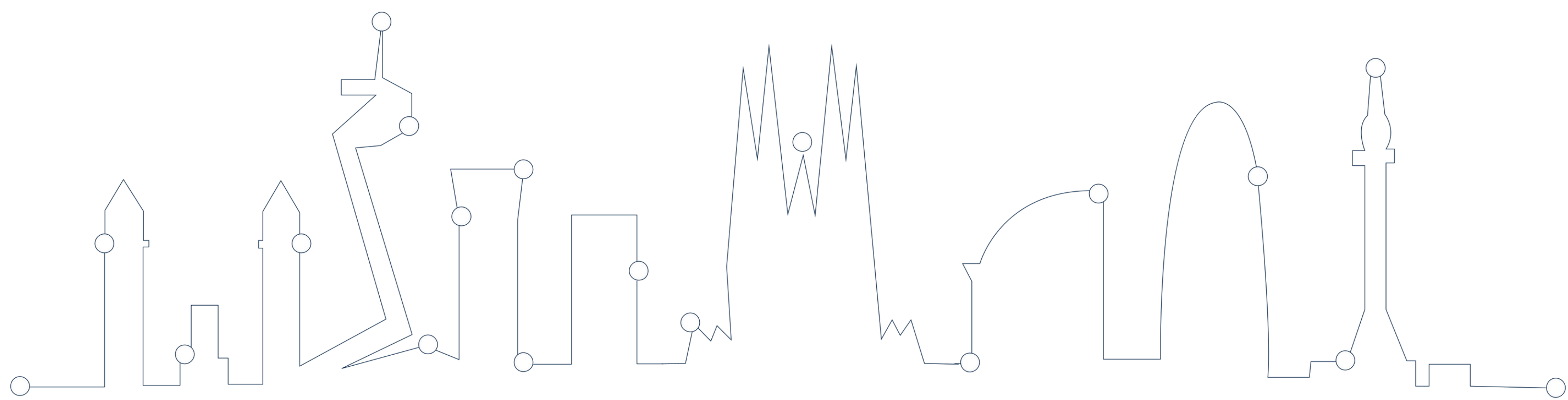
We are working together with leading companies and partners in the field, both international and European, under initiatives like Digital Autonomy with RISC-V in Europe (DARE) the European Processor Initiative (EPI).



Advancing European Technological Sovereignty:

Our primary goal is to reduce Europe's dependence on foreign hardware technologies, strengthening its capacity to produce critical technology internally.

This initiative is part of a broader strategy, including the “PERTE Chip” aimed at positioning Spain as a leader in the design and manufacture of advanced microprocessors and alternative architectures.



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Plan de
Recuperación,
Transformación
y Resiliencia



**Barcelona
Supercomputing
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