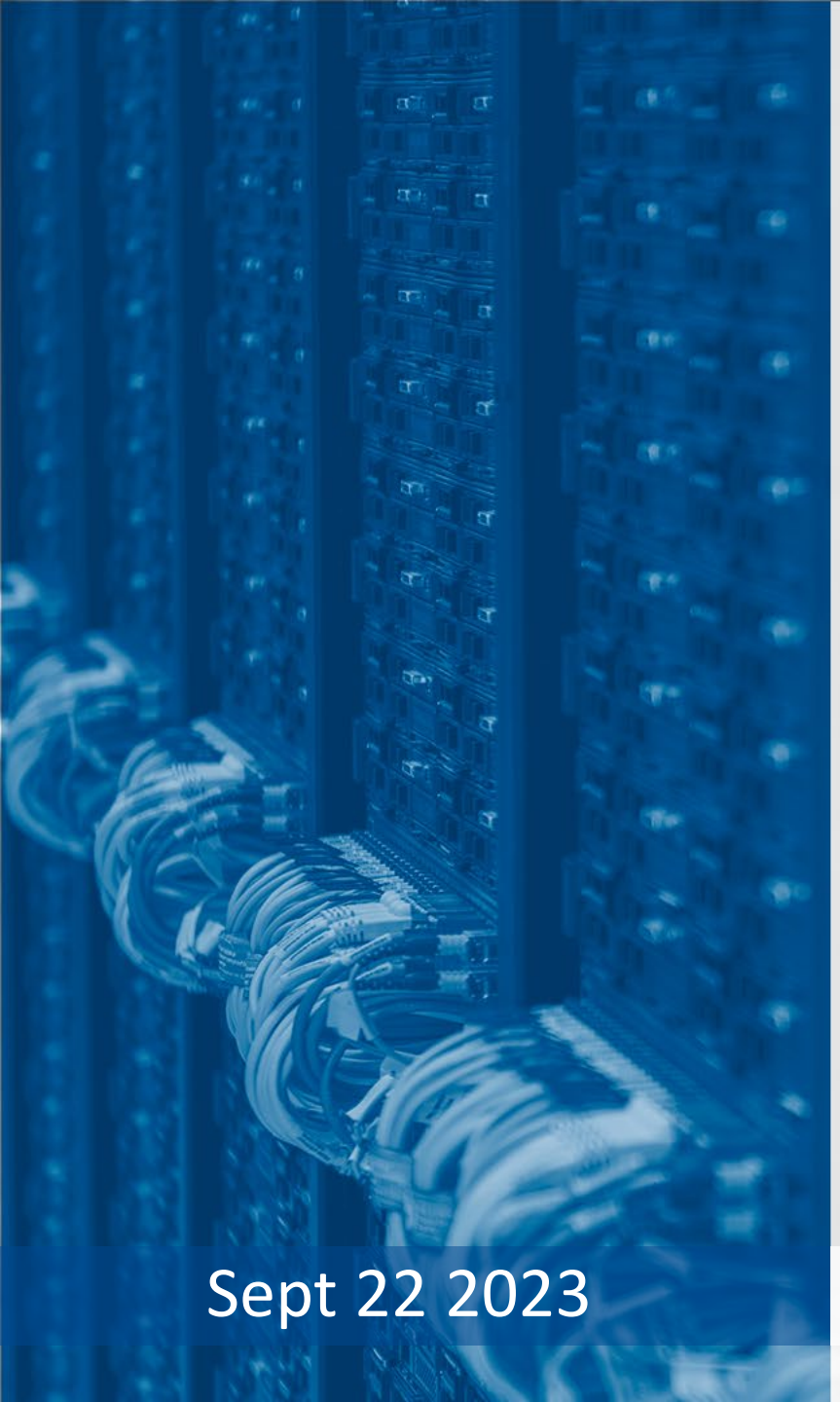

Barcelona Supercomputing Center
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Designing High Performance Computers at the Barcelona Supercomputing Center

Rafael Gomà

BSC

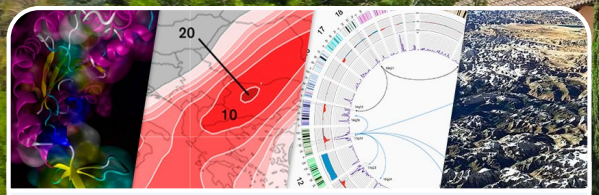
Sept 22 2023

BSC, Barcelona (Spain)

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

MareNostrum 5 (314Pflops)

Supercomputing services
to Spanish and EU researchers



R&D in Computer, Life, Earth
and Engineering Sciences

PhD programme, Tech
transfer, public engagement

Application dept.

BSC-CNS is a consortium that includes

Spanish Government	60%
Catalan Government	30%
Univ. Politècnica de Catalunya (UPC)	10%

MareNostrum 5

Total peak performance: **314** Pflops

PRACE

Access: prace-ri.eu/hpc_acces

RES
RED ESPAÑOLA DE SUPERCOMPUTACIÓN

Access: bsc.es/res-intranet

BSC Barcelona Supercomputing Center
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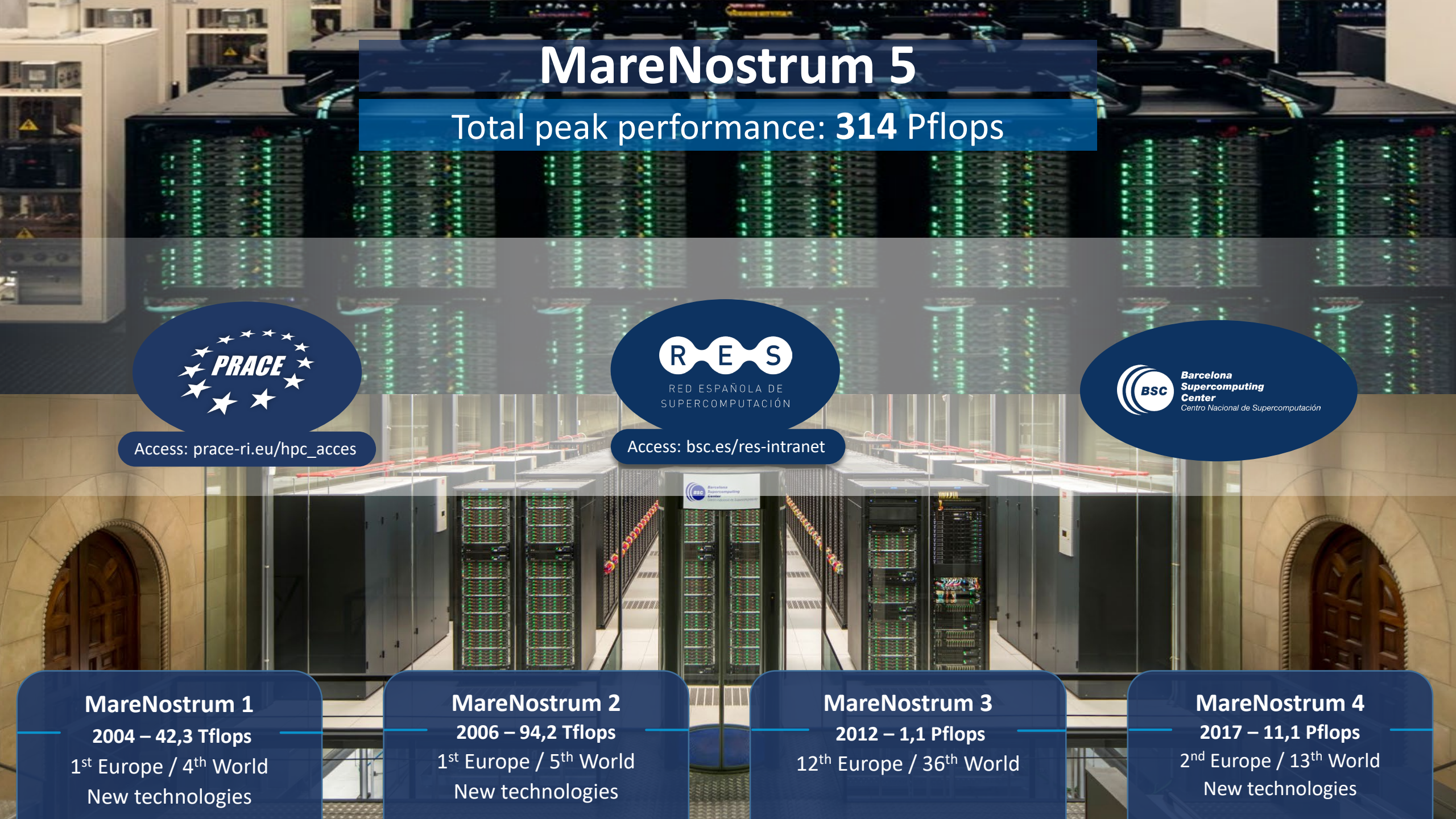
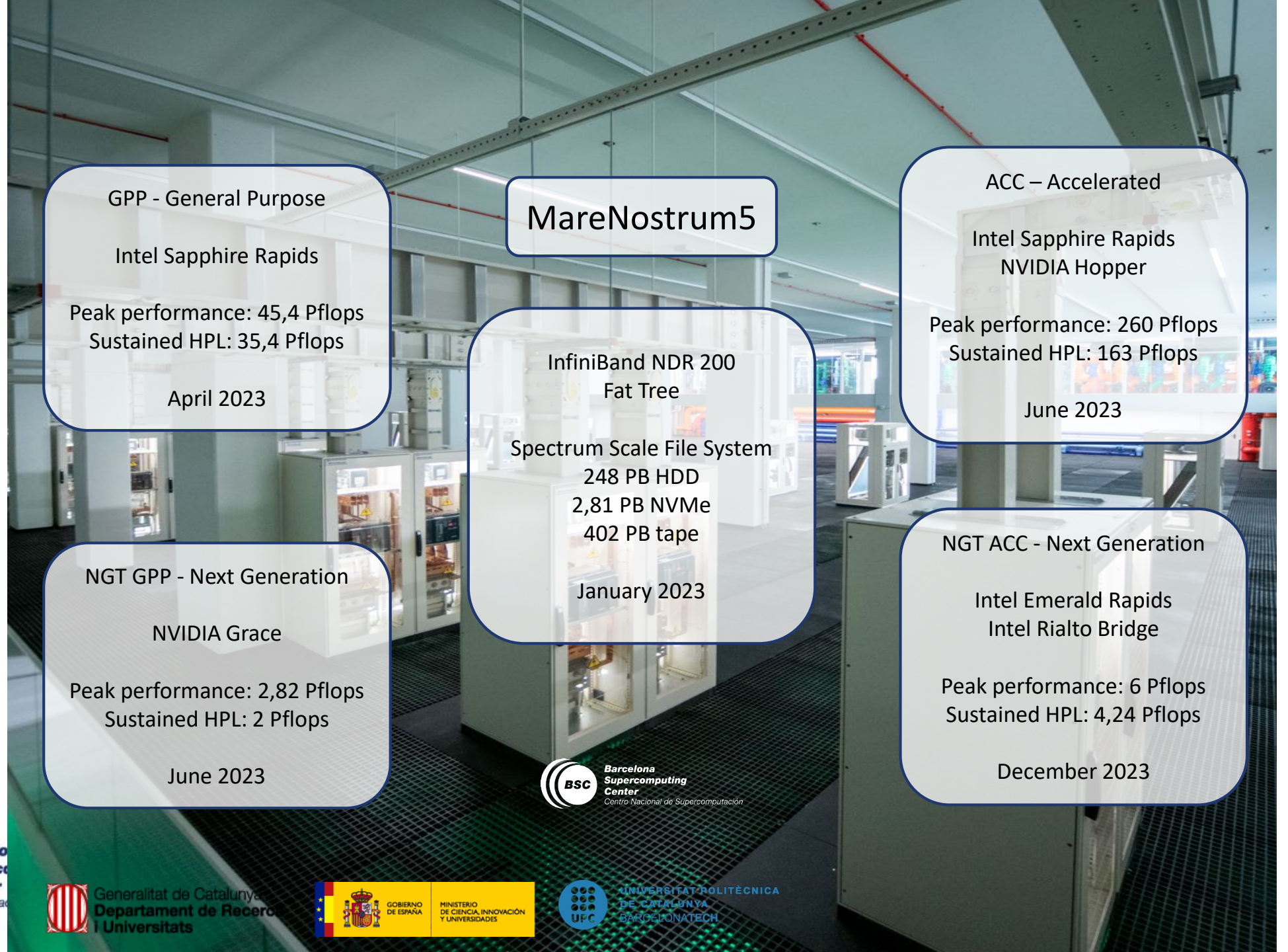


MareNostrum 1
2004 – 42,3 Tflops
1st Europe / 4th World
New technologies

MareNostrum 2
2006 – 94,2 Tflops
1st Europe / 5th World
New technologies

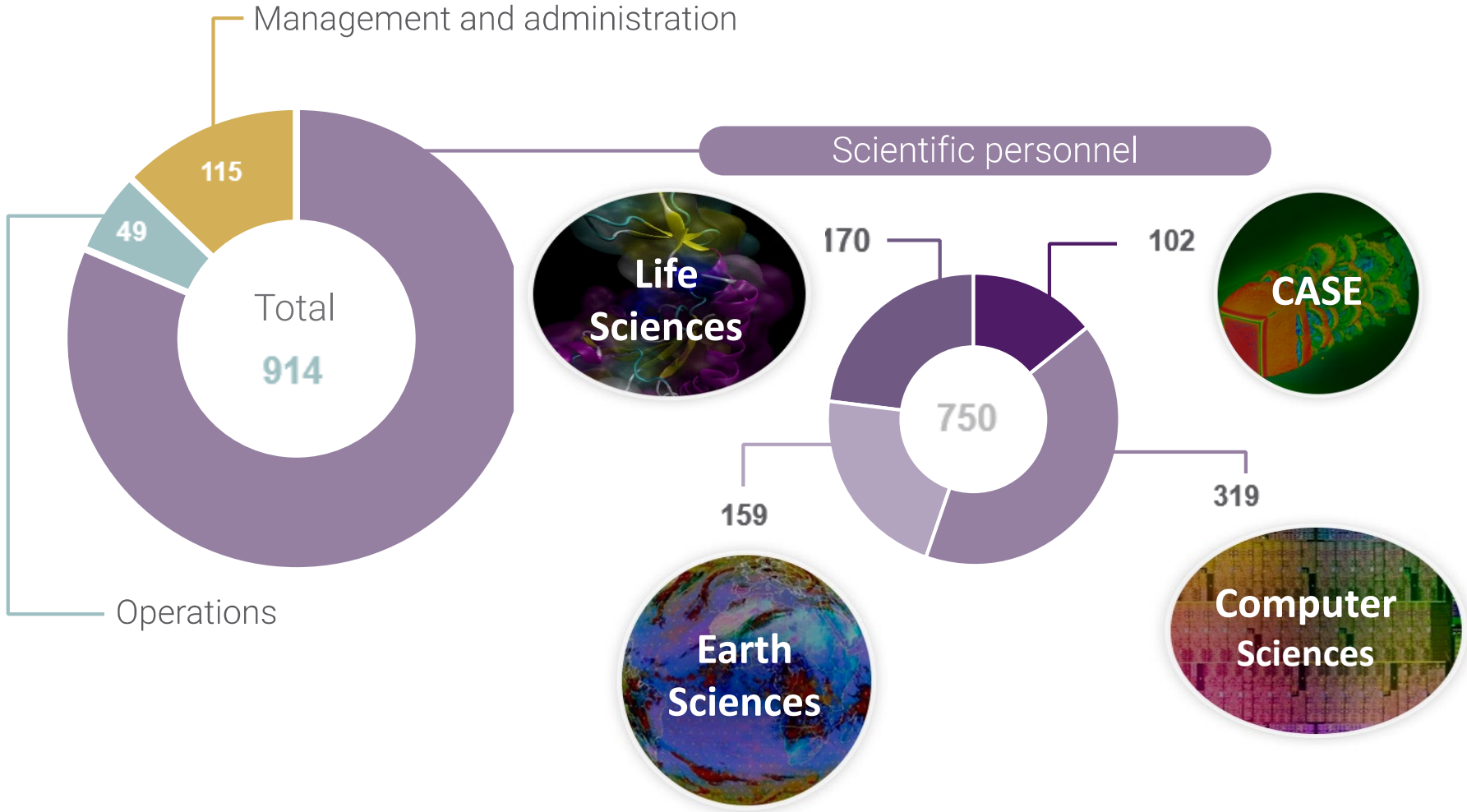
MareNostrum 3
2012 – 1,1 Pflops
12th Europe / 36th World

MareNostrum 4
2017 – 11,1 Pflops
2nd Europe / 13th World
New technologies


MareNostrum5
GPP - General Purpose
Intel Sapphire Rapids
Peak performance: 45,4 Pflops
Sustained HPL: 35,4 Pflops
April 2023
InfiniBand NDR 200
Fat Tree
Spectrum Scale File System
248 PB HDD
2,81 PB NVMe
402 PB tape
January 2023
ACC – Accelerated
Intel Sapphire Rapids
NVIDIA Hopper
Peak performance: 260 Pflops
Sustained HPL: 163 Pflops
June 2023
NGT GPP - Next Generation
NVIDIA Grace
Peak performance: 2,82 Pflops
Sustained HPL: 2 Pflops
June 2023
NGT ACC - Next Generation
Intel Emerald Rapids
Intel Rialto Bridge
Peak performance: 6 Pflops
Sustained HPL: 4,24 Pflops
December 2023
BSC
Barcelona Supercomputing Center
Centro Nacional de Supercomputación

BSC in numbers

People



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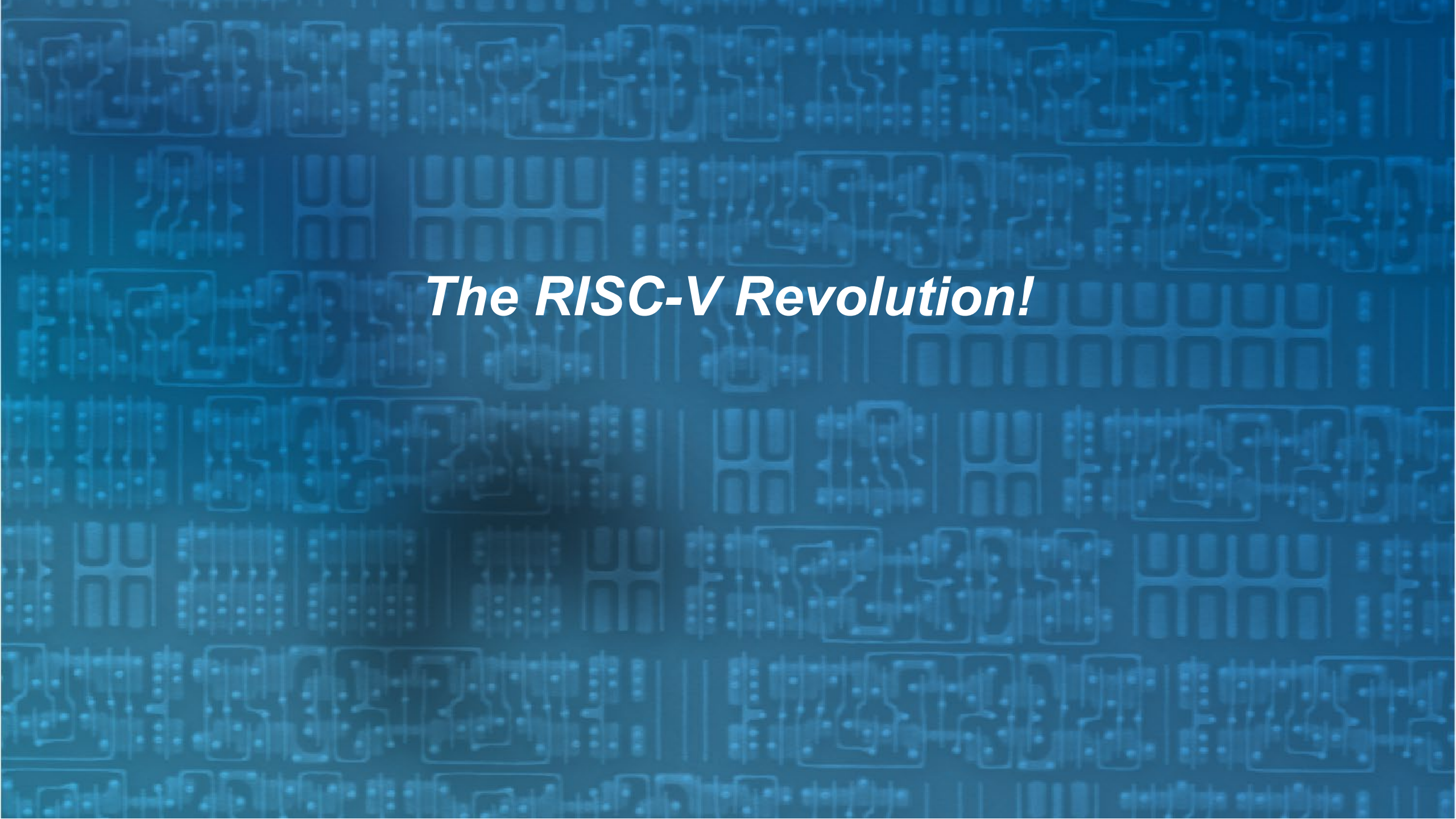
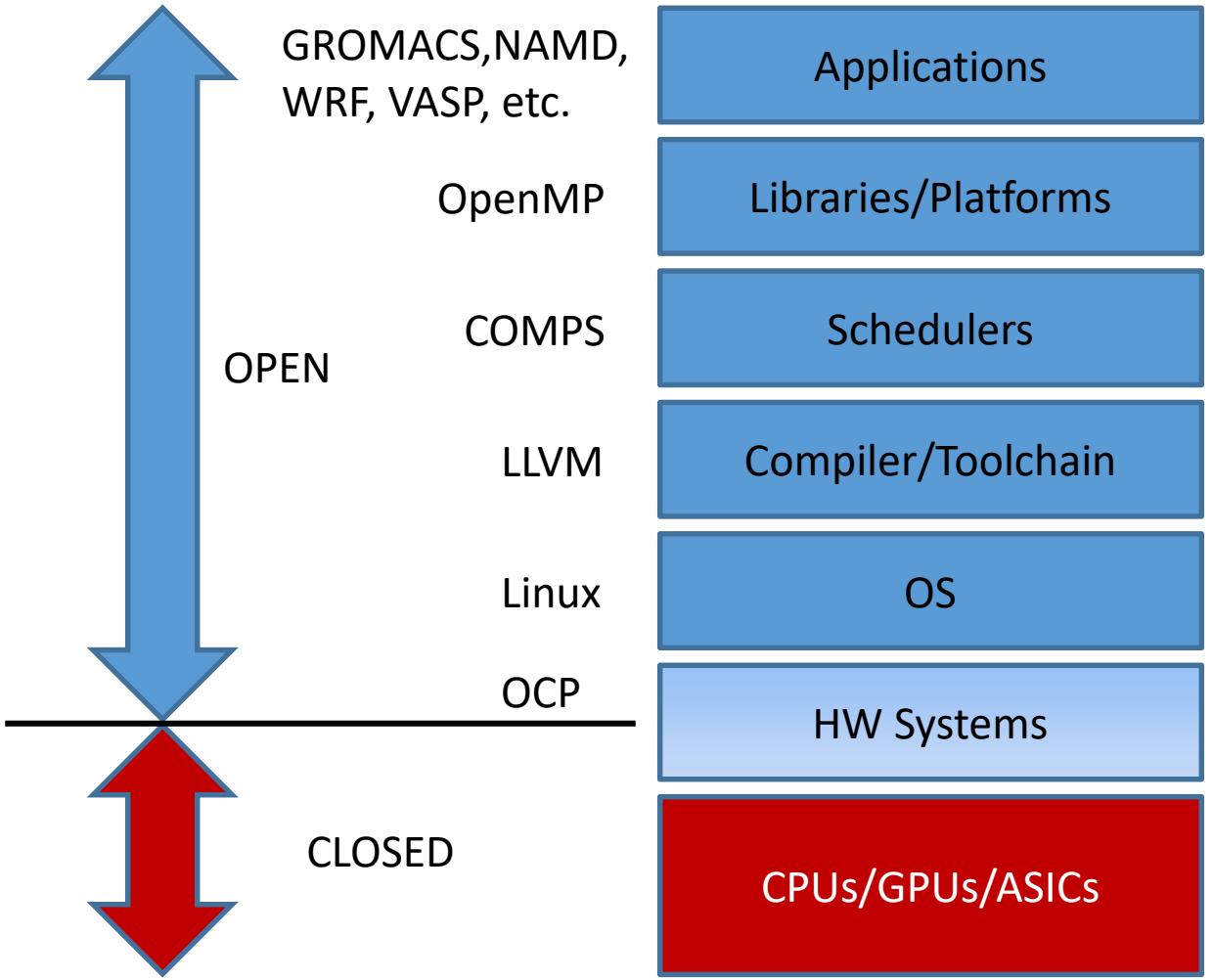
Data as of July 31st, 2023


The RISC-V Revolution!

HPC Today

- **Europe has led the way in defining a common open HPC software ecosystem**
- **Linux** is the de facto standard OS despite proprietary alternatives
- Software landscape from Cloud to IoT already enjoys the benefit of open source
- Open source provides:
  - A common platform, specification and interface
  - Accelerates building new functionality by leveraging existing components
  - Lowers the entry barrier for others to contribute new components
  - Crowd-sources solutions for small and larger problems
- **What about Hardware and in particular, the CPU?**



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RISC-V is an Open Standard Instruction Set Architecture (ISA)

Software uses the ISA to tell the hardware what to do.

At the base level, the RISC-V ISA and extensions ratified by RISC-V International are royalty free and open base building blocks for anyone to build their own solutions and services on.

RISC-V International is the global non-profit home of the open standard RISC-V ISA, related specifications, and stakeholder community

RISC-V®

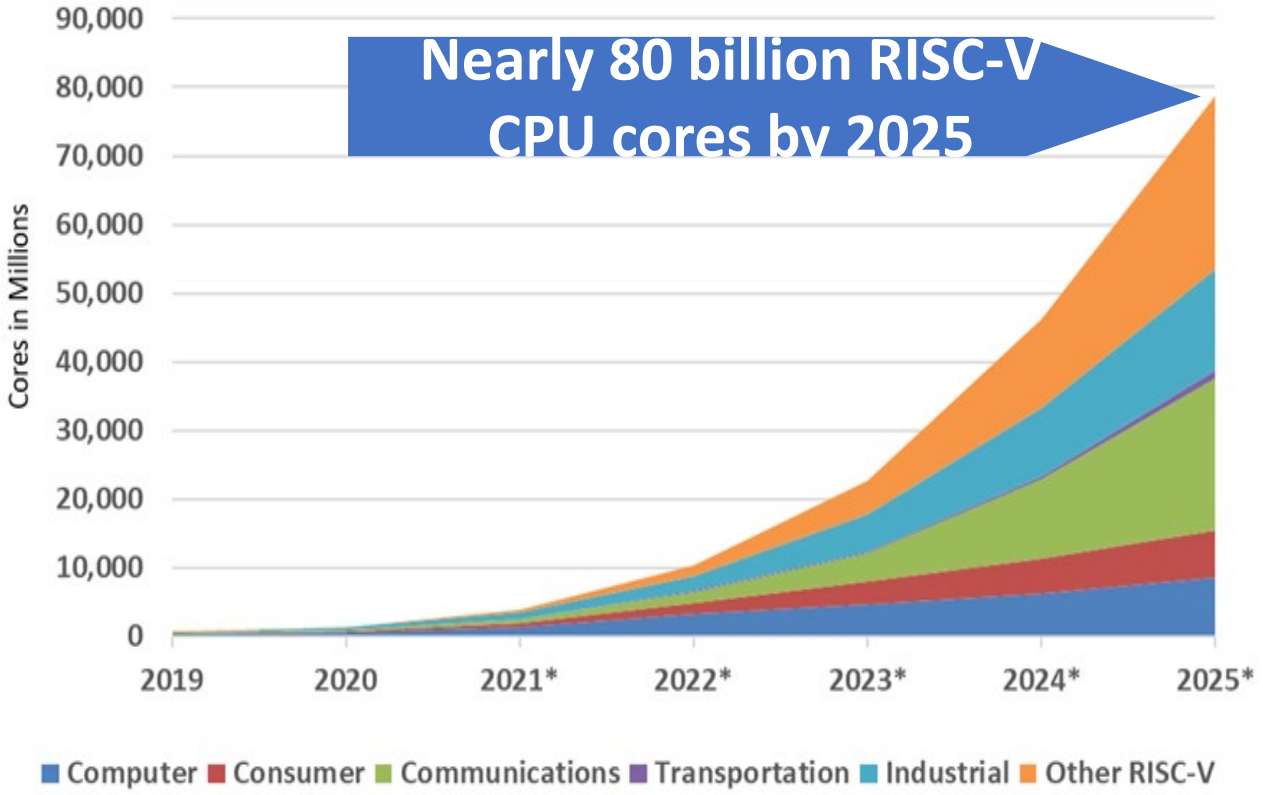
RISC-V is rapidly building the strongest ecosystem

RISC-V instrumented with software top of mind

- **Open standards enable software choice** Applications keen to run on RISC-V.
- **Toolchain and OS support** required for Extension ratification
- **Single hypervisor standard** to simplify and unify application support
- **Thousands of software developers** bringing workloads to RISC-V
- **Strategic imperative and investment** by commercial sector and geographies
- **Modern design approaches** leveraged for fewer instructions

Barcelona Supercomputing

RISC-V CPU core market grows 114.9% CAGR, capturing >14% of all CPU cores by 2025

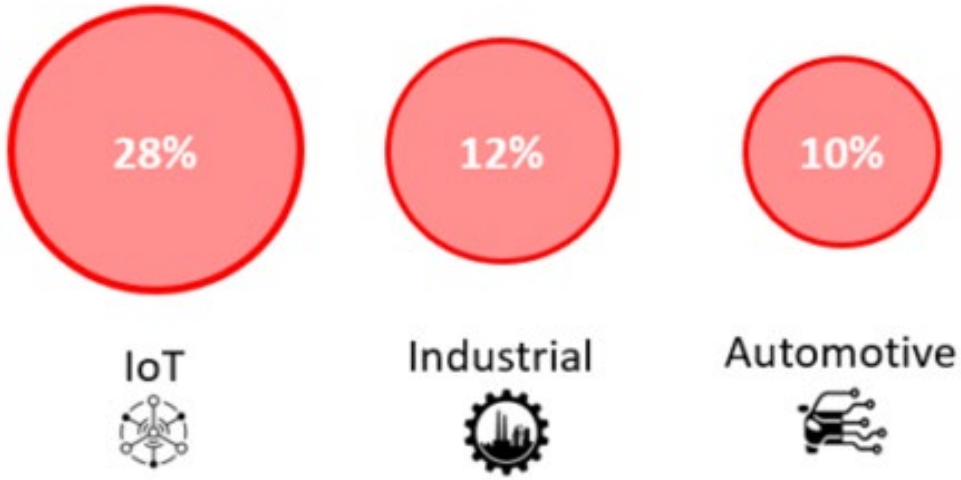


Barcelona Supercomputing Center
Centro Nacional de Supercomputación

RISC-V®

Source: Semico Research Corp, March 2021

RISC-V Penetration Rate by 2025



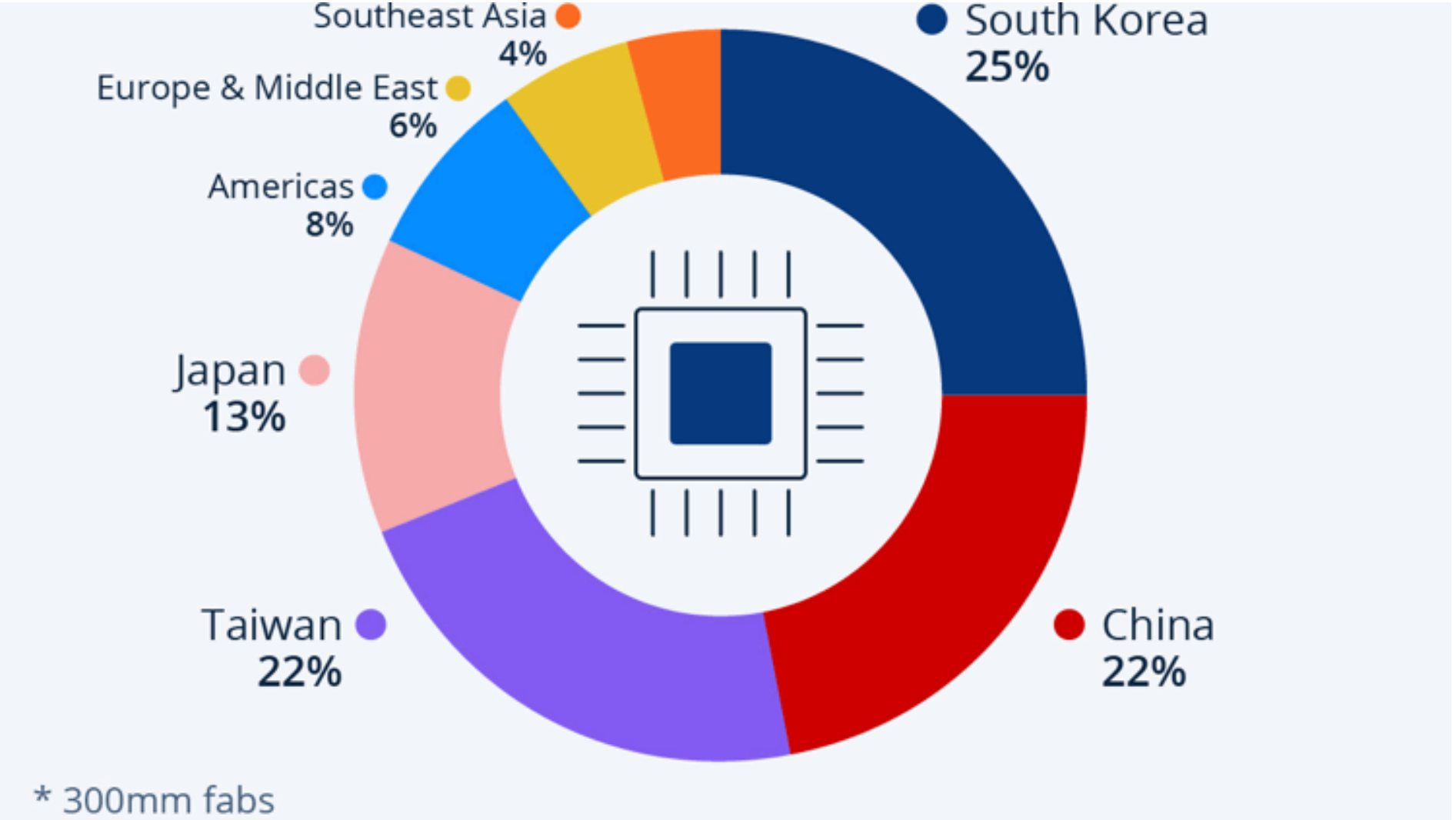
“The rise of RISC-V cannot be ignored... RISC-V will shake up the $8.6 Billion semiconductor IP market.”

-- William Li, Counterpoint Research

Source: Counterpoint Research, September 2021

The European Processor Initiative (EPI)

WW Semiconductors market



Microprocessor Technology: Strategy

EU goal: autonomy in strategic processing technologies

EuroHPC
Joint Undertaking

*Our **ambition:** by 2030*

- *The production of cutting-edge and sustainable semiconductors in Europe including processors is at least **20% of world production** in value*
- *Manufacturing capacities below **5nm** nodes aiming at 2nm*
- ***Energy efficiency** 10X more than today*

✓ ***RISC-V ISA plays a central role on EU's technology strategy***

The European Processor Initiative

The European Processor Initiative (EPI) under the SGA1 of the Framework Partnership Agreement (FPA: 800928), to design and implement a roadmap for a new family of low-power European processors for extreme scale computing, high-performance Big-Data and a range of emerging applications.

- **History:** Remember MontBlanc? BSC leads the RISC-V HPC accelerator development
- **Consortium (SGA1):**

28 partners from 10 European countries to Coordinate: Bull SAS (France)

- **Budget:** €80M (100% funded)
- **Duration:** 36 months (01/12/2018-31/12/2021)
- **5 Streams** (4 Technical and 1 Management/Exploitation/C&D)

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

Key contact point

☞ Jesús Labarta jesus.labarta@bsc.es

EPI MAIN OBJECTIVE

To develop European microprocessor and accelerator technology

- Strengthen competitiveness of EU industry and science

SiPearl

Rhea

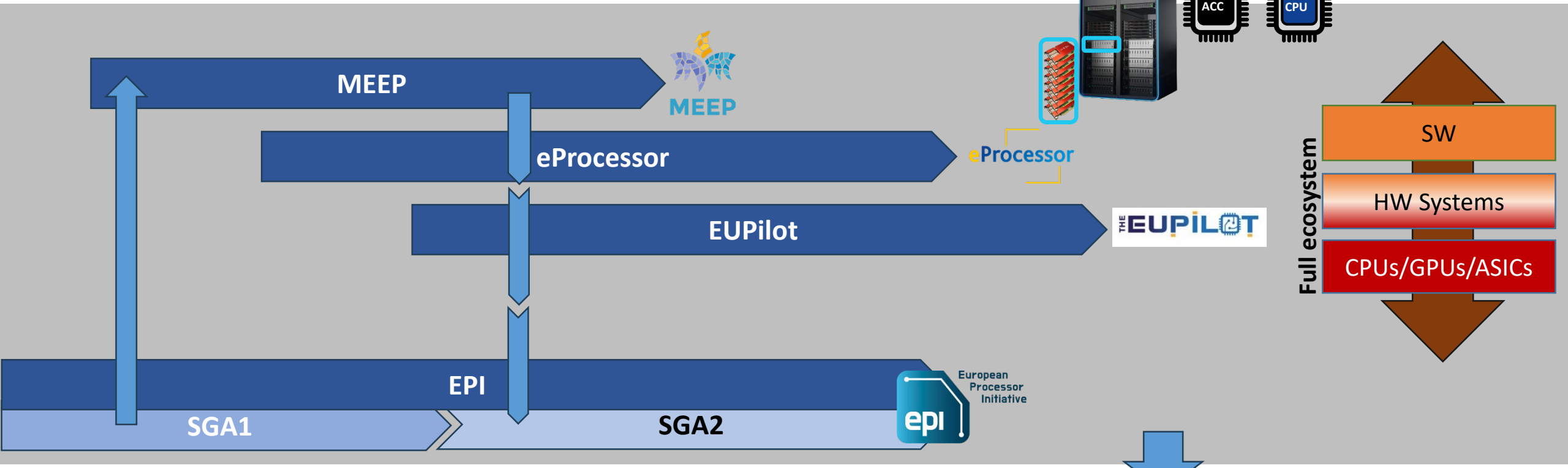
Arm-based general purpose CPU

EPAC

RISC-V based Accelerators

BSC, SemiDynamics, EXTOLL, FORTH, ETHZ, UniBo, UniZG, Chalmers, CEA, E4, Menta, ZPT, …

RISC-V@BSC: EU Projects



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DRAC Project

- **DRAC**: **D**esigning **R**ISCV-based **A**ccelerators for next generation **C**omputers
  - Consortium: BSC (coord.), UPC, UAB, UB, URV
  - Dates: June 2019 – June 2023
  - Budget: 4M€ (50% co-funded by Generalitat)
  - Alignment with the European Processor Initiative (EPI) project:
    - Focus on RISC-V-based accelerator developed in Barcelona
    - Promote RISC-V in the CS degrees in Catalan universities
    - Build IC design teams capable of taping out DRAC technology: RTL design, verification and physical design

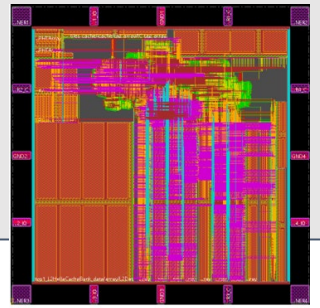
RIS3CAT
Research and Innovation Strategies for Smart Specialisation a CATALUNYA

UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH
Facultat d'Informàtica de Barcelona
BSC Barcelona Supercomputing Center Centro Nacional de Supercomputación
UNIVERSITAT DE BARCELONA
BSC Barcelona Supercomputing Center Centro Nacional de Supercomputación
UAB Universitat Autònoma de Barcelona
UNIVERSITAT ROVIRA I VIRGILI

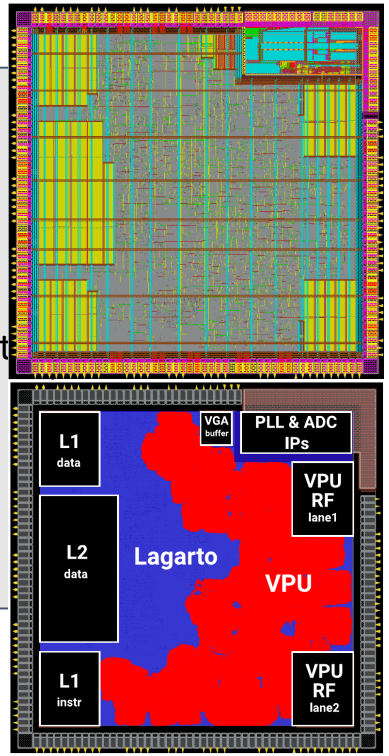
Lagarto RISC-V Tapeouts

2019 2020 2021 2022 2023

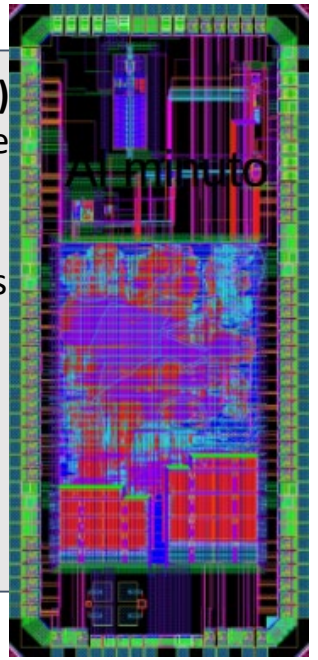
Lagarto (May'19)
- Lagarto Hun 5-stage in-order
- 150MHz (external)
- TSMC 65nm
- 2.5mm2



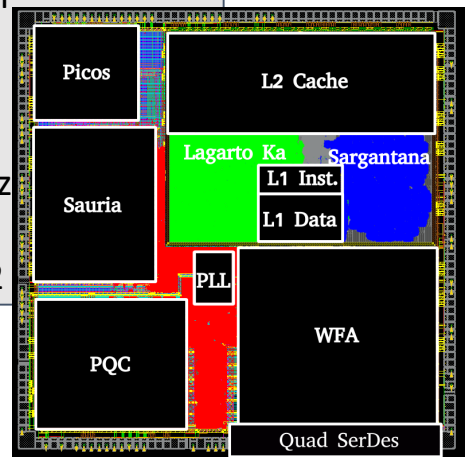
DVINO (Apr'21)
- Lagarto Hun in-order
- VPU
- PLL 600 MHz
- SDRAM mem cont
- HyperRAM
- VGA
- ADC
- TSMC 65nm
- 8mm2



Sargantana (Feb'22)
- Sargantana 7-stage in-order
- PLL 1.2 GHz
- Custom extensions
- SDRAM
- Prototype analog IPs: SerDes 8GHz
- GF 22nm
- Area: 2.9mm2



Kameleon (Dec'22)
- Lagarto Ka 11-stage ooo
- PLL 1.2 GHz
- Automotive Accel
- Crypto Accel
- Genomic Accel
- PICOS Accel
- SerDes 8GHz
- GF 22nm
- Area: 9mm2



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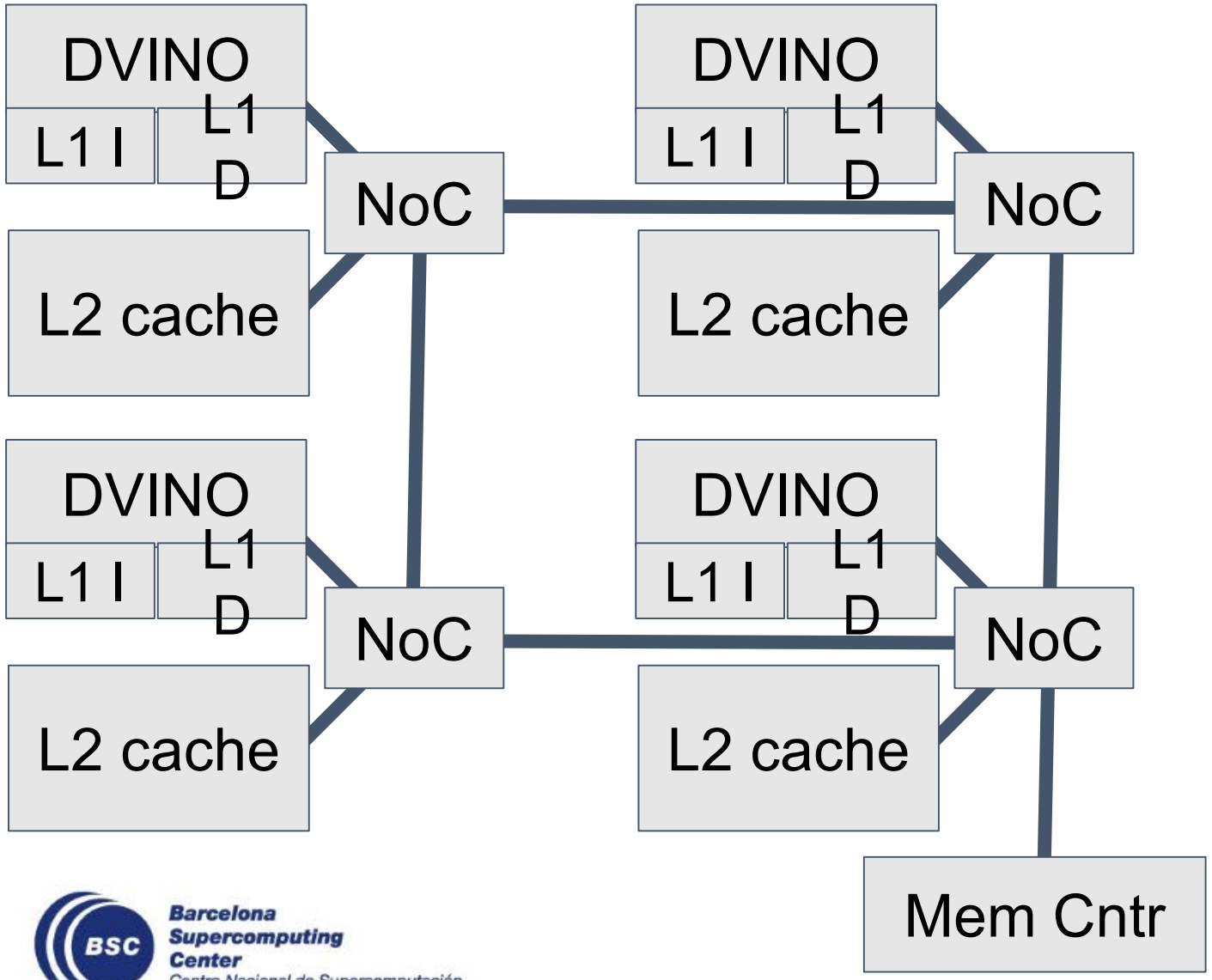
First Steps Towards a Lagarto Multicore



- Multicore design based on:
  - DVINO processor
  - RISC-V ISA support: I, M, A, F, D, C, V
  - 4-lane VPU
  - OpenPiton 2-level cache hierarchy (priv. L1, shared L2)
- Current status
  - Linux boot (openSBI)
  - RTL simulation of parallel applications (up to 64 cores)
  - Multiple memory controllers
  - FPGA-ready
  - Integrating Ka+VPU

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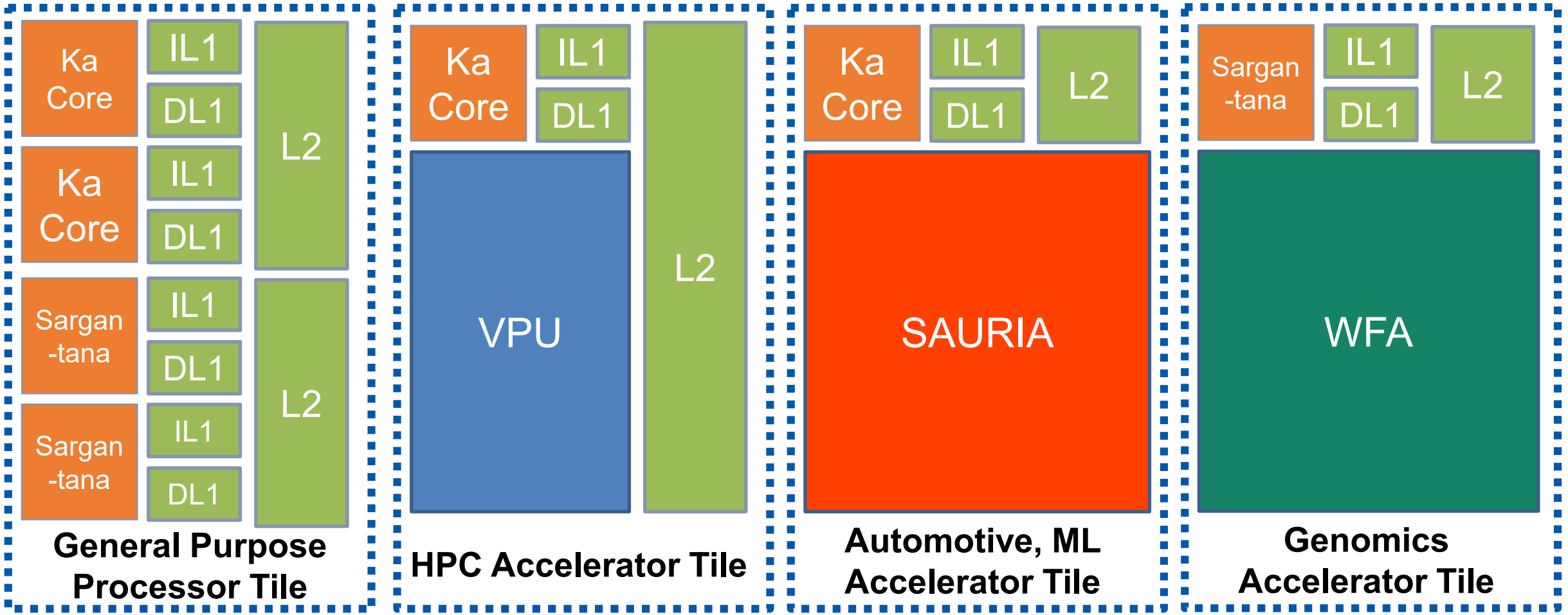
European Processor Initiative

MEEP
MareNostrum Experimental Exascale Platform

Towards a RISC-V Heterogeneous Manycore



Other Domain-Specific Accelerator Tiles (sparse, security, safety, etc.)

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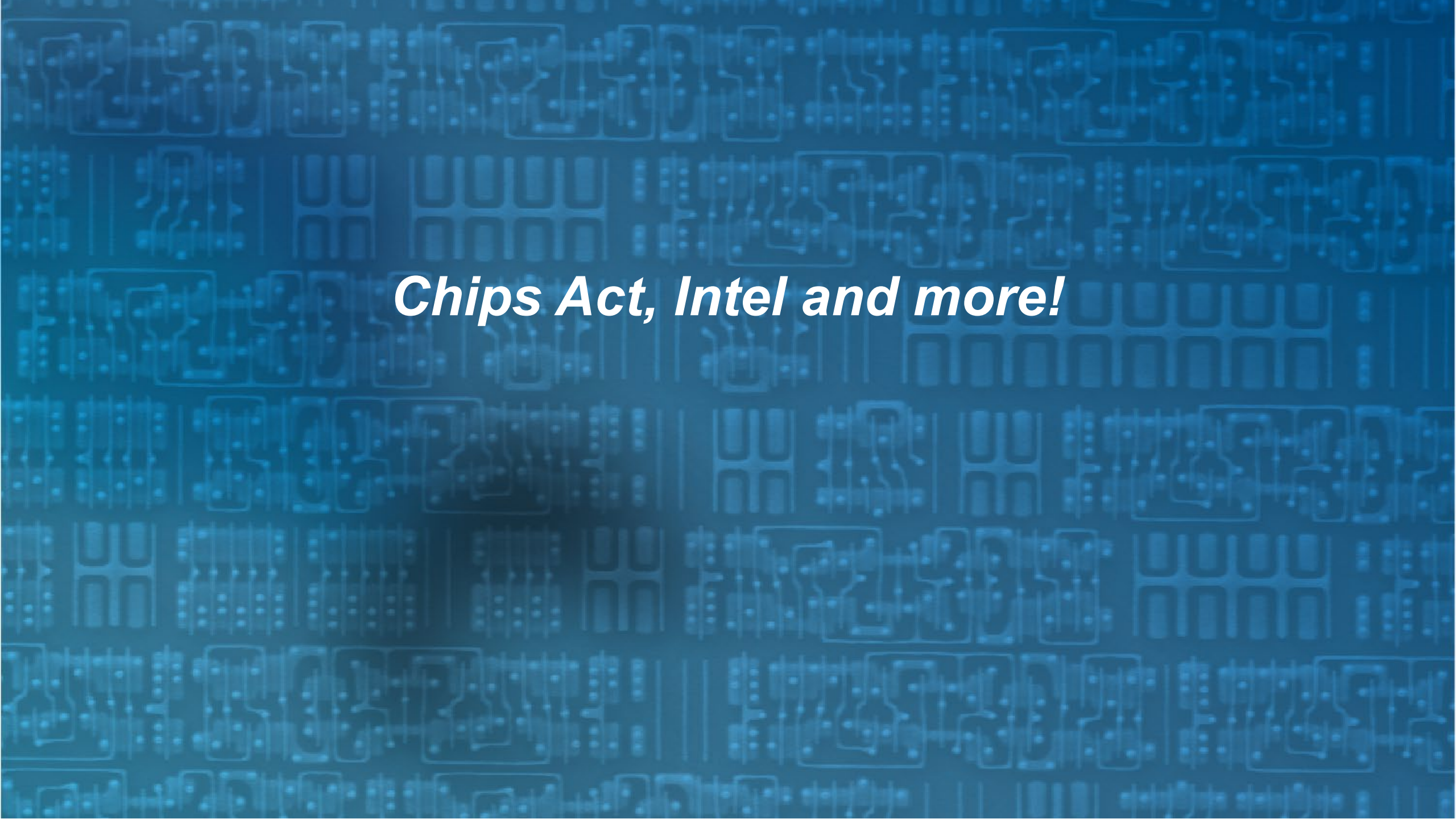
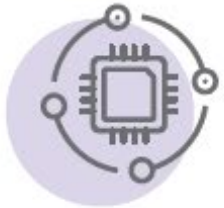

Chips Act, Intel and more!

EUROPEAN CHIPS ACT

The European Chips Act will ensure that the EU strengthens its semiconductors ecosystem, increases its resilience, as well as ensure supply and reduce external dependencies.

1. Strengthen Europe's research and technology leadership towards smaller and faster chips



2. Build and reinforce capacity to innovate in the design, manufacturing and packaging of advanced chips

3. Put in place a framework to increase production capacity to 20% of the global market by 2030

4. Address the skills shortage, attract new talent and support the emergence of a skilled workforce

5. Develop an in-depth understanding of the global semiconductor supply chains

The Chips Act should result in additional public and private investments of more than **€15 billion**.

These investments will complement:

- **existing programmes** and actions in research & innovation in semiconductors (Horizon Europe, Digital Europe programme)
- **announced support** by Member States.

In total, **more than €43 billion of policy-driven investment will support the Chips Act until 2030**, which will be broadly matched by long-term private investment.

3. EXECUTION
ACTIONS & BUDGET (I)

	M€
COMPONENT I. BOLSTERING SCIENTIFIC CAPACITY	**1.165**
ACTION 1: Development of R&D&i on cutting-edge and alternative architecture microprocessors	475
ACTION 2: Development of R&D&i on integrated photonics	150
ACTION 3: Development of R&D&i on quantum chip development	40
ACTION 4: Budget line for the IPCEI on Microelectronics and Communication Technologies	500
COMPONENT II. DESIGN STRATEGY	**1.330**
ACTION 5: Creation of cutting-edge alternative architecture microprocessor fabless companies	950
ACTION 6: Creation of pilot lines	300
ACTION 7: Creation of a network for education, training and skills-building in relation to semiconductors	80

3. EXECUTION
ACTIONS & BUDGET (II)

	M€
COMPONENT III. CONSTRUCTION OF FABRICATION PLANTS IN SPAIN	**9.350**
ACTION 8: Creating fabrication capacity at sizes below 5 nm	7.250
ACTION 9: Creating fabrication capacity at sizes above 5 nm	2.100
COMPONENT IV. STIMULATING THE ICT MANUFACTURING INDUSTRY IN SPAIN	**400**
ACTION 10: ICT manufacturing industry incentive scheme	200
ACTION 11: Creation of a chips fund	200
GOVERNANCE	**5**
Special Commissioner for the Microelectronic and Semiconductors Project	5
TOTAL PUBLIC INVESTMENT	**12.250**

Intel Labs Barcelona are back!

- New joint Intel – BSC Laboratory to design HPC processors based on RISC-V technology
- Funding: 400M$ in the next 10 years. Headcount: ~200 (estimated)

Other companies will also come to Spain!

Path to Zettascale

Developing European Hardware/Software Technology

Full Stack Open Source HPC Ecosystem

Build Full System based on RISC-V: MN6 and many others

European & Global collaboration

Intel and BSC: Continuing to collaborate into the Zettascale era

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intel

Research & Product

Announced at ISC in June 2022

BSC is building a New Lab!
100+ Job Opportunities

Research Engineer/Researcher

R&D for Zettascale and beyond: Applications to Accelerators

If your experience and/or motivation include any of the disciplines and skills below, check out our QR:

Hardware (Processor architecture, micro-architecture, accelerators, memory hierarchy, memory controllers, HBM, DRAM, non-volatile memory, RTL design, VHDL, verilog, SystemC, System verilog, Synopsys, Cadence, Mentor Graphics, synthesis, place and route, timing closure, packaging, PCB design, verification, validation, CI, post-silicon debug, DFT, gate-level simulation,…)

Software (programming models, MPI, compilers (LLVM), SYCL, OneAPI, Tensorflow, PyTorch, Apache Spark, CI/CD, operating systems, managed runtimes, OpenMP, task-based programming models, containers, security, fault-tolerance, virtualization, C/C++, Tcl, Python, Perl/Csh,…)

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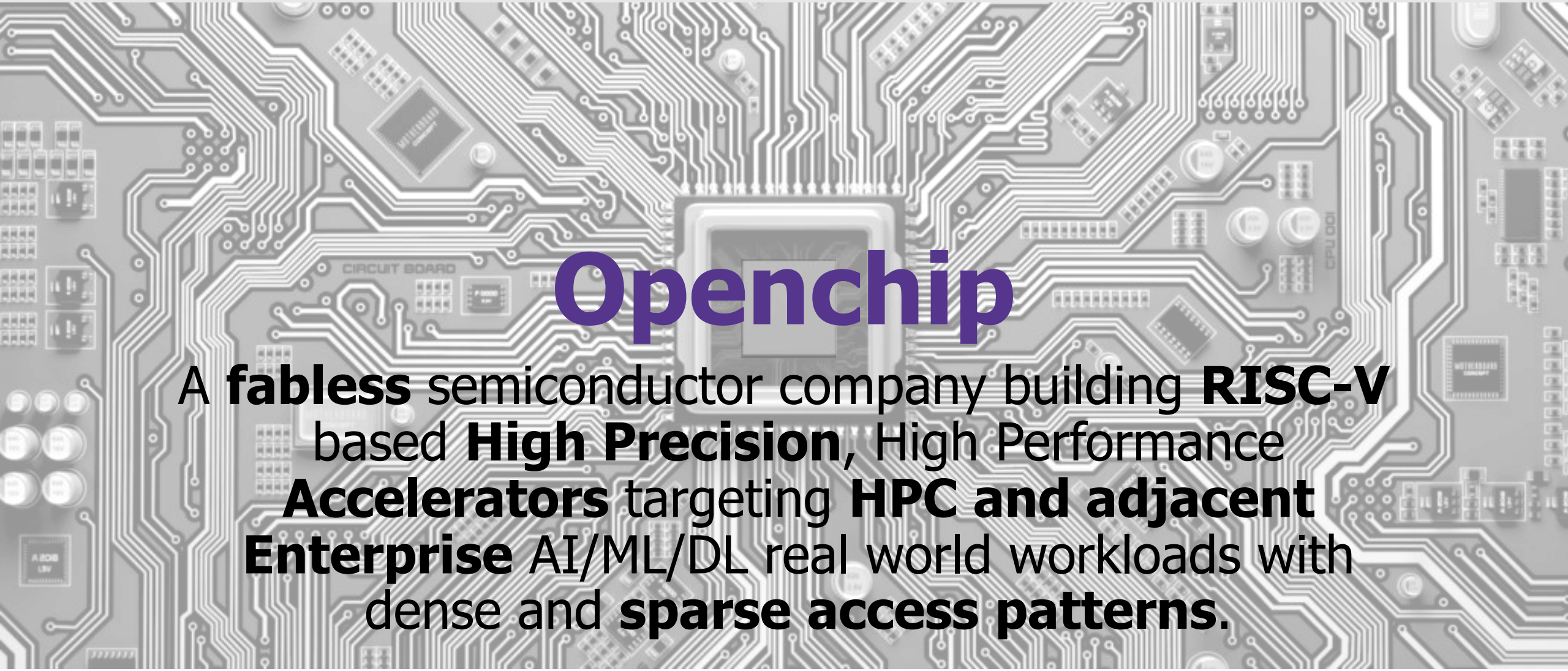
Reference: 176_23_CS_Z_R0-4-RE1-4



Openchip

A **fabless** semiconductor company building **RISC-V** based **High Precision**, High Performance **Accelerators** targeting **HPC and adjacent Enterprise** AI/ML/DL real world workloads with dense and **sparse access patterns**.

Spanish Open Hardware Alliance

29 Universities and 3 research centers are partnering to share proposals and collaborate to take advantage of the opportunity raised by the global adoption of the **RISC-V standard.**
Also, establishing bridges with related industry associations like AESEMI

Without universities, there is nor talent neither chips!